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HSF Property:ROHS

ACER

BAP41/BAP51/BAP52/BXP41/SJM52

UMA+Discrete(SW Gfx)

MAIN BOARD

2009.06.30

Tuesday, June 30, 2009		A02
DATE	CHANGE NO.	REV

	EE	DATE	POWER	DATE	INVENTEC			
DRAWER					TITLE			
DESIGN					BAP41/BAP51 (Montevina SFT)			
CHECK					SIZE			
RESPONSIBLE					C			
SIZE					VER:			
FILE NAME: XXXX-XXXXXXX-XX					C			
PIN XXXXXXXXXXXXX					SHEET			
					1 of 48			

1. Schematic Page Description :

Montevina Schematic Ver : A02

1. Title

2. Schematic Page DESCR

3. Block Diagram

4. Annotations

5. Schematic Modify

6. Timing Diagram

7. Power Block Diagram

8. Adaptor in/Charge

9. 5VLA/5VA/3VA

10. 3VS/5VS/1.5V (DDR3)

11. 1.05VS/1.5S/1.8V/1.5VA

12. Power Latch/1.5VS/SCREW HOLE

13. CPU Core Power

14. GPU Core Power

15. Penryn Processor(1/2)

16. Penryn Processor(2/2)

17. CPU Thermal

18. Cantiga Host(1/6)

19. Cantiga DMI/Graph(2/6)

20. Cantiga DDRIII(3/6)

21. Cantiga Power(4/6)

22. Cantiga Power(5/6)

23. Cantiga Ground(6/6)
24. Clock Generator

25. DDR3 SDRAM SO-DIMM0

26. DDR3 SDRAM SO-DIMM1

27. ICH9M CPU/SATA(1/4)

28. ICH9M PCI/PCIE/DMI/USB(2/4)

29. ICH9M GPIO(3/4)

30. ICH9M Power/GND(4/4)

31. LCD/CRT

32. KBC ITE8502E-L

33. IO CN

34. IO CN

35. IO CN

36. Audio Codec

37. EASY PORT CN/ LEVEL SHIFTER

38. M92-S2(1/5)

39. M92-S2(2/5)

40. M92-S2(3/5)

41. M92-S2(4/5)

42. M92-S2(5/5)

43. DDR3 VRAM

44. HyBrid Switch

45. dGPU Power

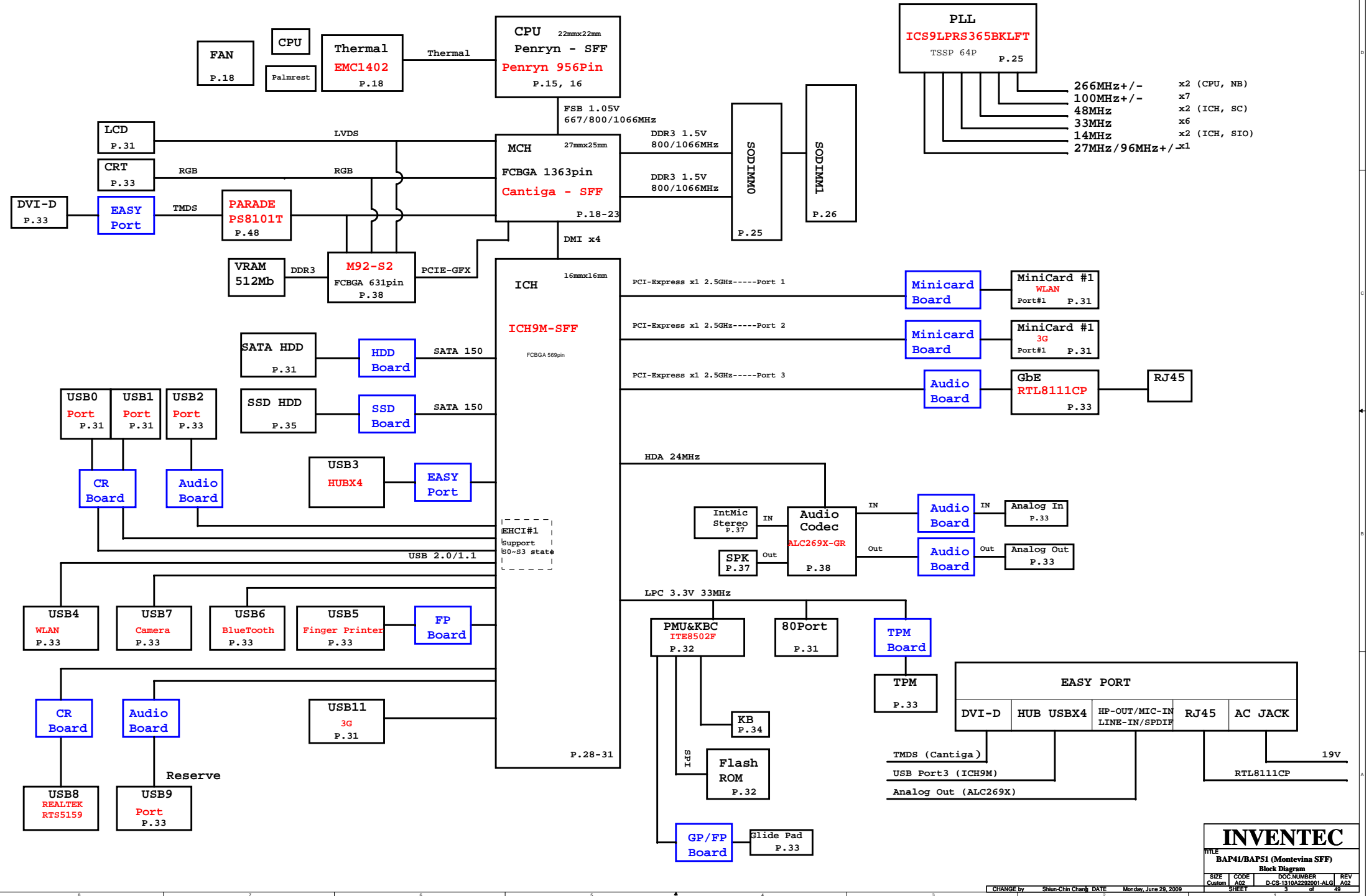
46. dGPU Power

47. dGPU Power

48. HDD Board

49. TPM Board

3. Block Diagram :



4. Net name Description :

Voltage Rails

DCIN	Primary DC system power supply
+5VLA	5.0V always on power rail by LATCH or ACIN
+5VA	5.0V always on power rail by ECPWON
+3VA	3.3V always on power rail by ECPWON
+5VS	5.0V switched power rail by SLP_S3#_3R
+3VS	3.3V switched power rail by SLP_S3#_3R
+1.8VS	1.8V switched power rail by SLP_S3#_3R
VCC_CORE	Core Voltage for CPU
+1.05VS	1.05V power rail for AGTL+ termination/Core for GMCH by SLP_S3#_3R
+1.25VS	1.25V switched power rail by SLP_S3#_3R
+1.5VS	1.5V power rail for CPU PLL/DMI/PCIE;DDRIII DLLs for GMCH/Core;PCIE for ICH9m by SLP_S3#_3R
+1.5V	1.5V power rail for DDRII by SLP_S5#_3R
0.75VDDT_DDRIII	0.75V DDRII Termination Voltage by SLP_S3#_3R

Part Naming Conventions

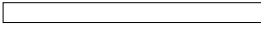



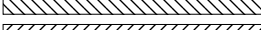



C	=	Capacitor
CN	=	Connector
D	=	Diode
F	=	Fuse
L	=	Inductor
Q	=	Transistor
R	=	Resistor
RP	=	Resistor Pack
U	=	Arbitrary Logic Device
Y	=	Crystal and Osc

Net Name Suffix

#	=	Active Low signal
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5. Board Stack up Description

PCB Layers

Layer 1		Component Side, Microstrip signal Layer
Layer 2		Ground Plane
Layer 3		Stripline Layer
Layer 4		Power Plane
Layer 5		Stripline Layer
Layer 6		Stripline Layer
Layer 7		Ground Plane
Layer 8		Solder Side, Microstrip signal Layer

	Differential Impedance for Microstrip	Differential Impedance for Stripline
Host Clock	95 ohm +/- 20%	95 ohm +/- 20%
PCI-E Clock	95 ohm +/- 20%	95 ohm +/- 20%
DDR3 CLK	75 ohm +/- 20%	75 ohm +/- 20%
DDR3 Strobe	90 ohm +/- 20%	90 ohm +/- 20%
DMI Bus	95 ohm +/- 20%	95 ohm +/- 20%
PCIE Bus	95 ohm +/- 20%	95 ohm +/- 20%
SDVO	95 ohm +/- 20%	95 ohm +/- 20%
SATA	95 ohm +/- 20%	95 ohm +/- 20%
USB	90 ohm +/- 20%	90 ohm +/- 20%
LVDS	95 ohm +/- 20%	95 ohm +/- 20%
Lan	95 ohm +/- 20%	95 ohm +/- 20%

Power Rail	Destination	Voltage	S0 Current
VCC_CORE	Penryn SFF HFM: LFM:	1.3319V-1.4375V-1.4591V 0.9221V-0.9625V-0.9739V	18A
1.05VS	Penryn SFF : AGTL+ termination Cantiga GS: Core Cantiga GS: PCIE Cantiga GS:Core+IMEL+HSIO Cantiga GS:VCC_GMCH Cantiga GS:VCCA_SM_CK and NCTF Cantiga GS:VCC_DMI Cantiga GS:VCCA_SM Cantiga GS:VTT ICH9M:VCC1_05 ICH9M:DMI ICH9M:CPU_IO	1V-1.05V-1.10V 0.997V-1.05V-1.102V 0.9975V-1.05V-1.1025V 0.9975V-1.05V-1.1025V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V 0.997V-1.05V-1.102V	4.5A 8.7A 1.78A 2.898A 10.154A 37.95mA 456mA 747.5mA 852mA 1.634A 48mA 2mA
1.5VS	Penryn SFF PLL Cantiga GS: QDAC Cantiga GS: LVDS Cantiga GS: TVDAC Cantiga GS: Various PLLS analog supply Cantiga GS: VCC_SM_CK Cantiga GS: VCC_SM ICH9M:PCIE_ICH ICH9M:SATA_ICH ICH9M:VCC_GLAN Mini Card: Express Card:	1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.71V-1.8V-1.89V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V 1.425V-1.5V-1.575V	130mA 0.5mA 60.31mA 35mA 485mA 149.5mA 3.1625A 646mA 1.342A 80mA 650mA
1.5V	Cantiga GS: DDRIII System Memory	1.425V-1.5V-1.575V	3.1A(800M) 4.1A(1067M)
0.75VDDT_DDRIII	DDRIII Terminator:	0.7125V-0.75V-0.7875V	1.0A
3VS	Cantiga GS: HV CMOS Cantiga GS: VCCS_TV DAC ICH9M:VCC3_3 ICH9M:VCCGLAN3_3 Thermal Sensor: Mini Card: UMTS Express Card: CLK Generator: ICS9LPRS365BKLFT Mini Card: WirelessLan Bluetooth: Super I/O: IT8305E Azalia Codec: ALC262 Azalia MDC:	3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.0V-3.3V-3.6V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.0V-3.3V-3.6V 3.0V-3.3V-3.6V	105.3mA 78mA 308mA 1mA 5mA 1.3A 500mA
1.8VS	DVI	3.0V-3.3V-3.6V	120mA
3VA	ICH9M: RTC ICH9M:VCCSUS3_3 ICH9M:VCCCL3_3 ICH9M:VCCLAN3_3 LCD: Lan:AR8131 Azalia MDC: Flash ROM: BIOS	2V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.135V-3.3V-3.465V 3.0V-3.3V-3.6V 3.0V-3.3V-3.6V 3.0V-3.3V-3.6V	6uA 212mA 73mA 78mA 2A 1A
5VS	Cardreader: RTS5159 Azalia Codec: ALC269 HDD: SATA ODD: SATA Audio AMP: G1432 Inverter: WebCam	3.0V-3.3V-3.6V 3.0V-3.3V-3.6V 4.75V-5.0V-5.25V 4.75V-5.0V-5.25V 4.75V-5.0V-5.25V 4.75V-5.0V-5.25V	Max: 1.5A ; R/W: 460mA ; STDBY: 70mA Max: 1.5A ; R/W: 900mA ; STDBY: 45mA
5VA	USB: x 2 ports USB	5VA 5VA	1A 2A 1.5A
5VLA	Control Power		
3VLA	EC: ITE8512E	3.0V-3.3V-3.6V	300mA

INVENTEC

FILE: BAP41/BAP51 (Montevina SFF)

ANNOTATIONS

SIZE	CODE	DOC NUMBER	REV
Custom	A02	D-CS-1310A222001-ALG	A02
SHEET	4	of	48

6.Schematic modify Item and History :

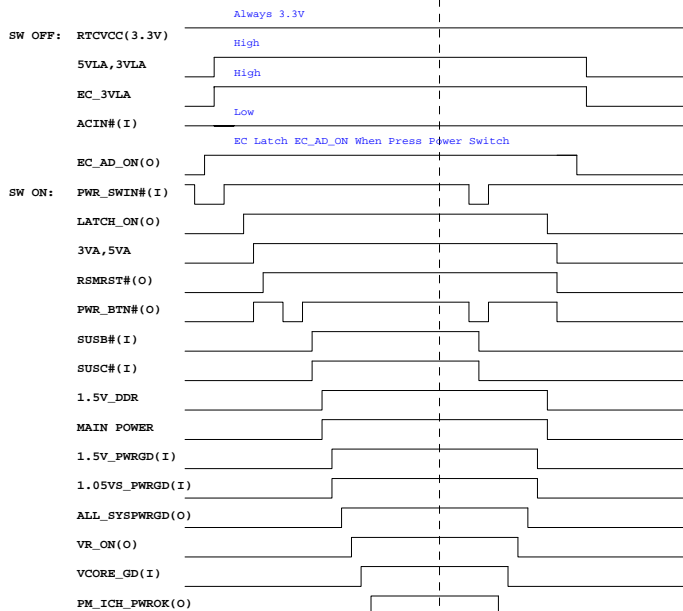
INVENTEC			
TITLE BAP41/BAP51 (Montevina SFF)			
Schematic Modify			
SIZE Custom	CODE A02	DOC NUMBER D-CS-1310A2282001-ALG	REV A02

SYSTEM POWER ON/OFF SEQUENCE

Drawing : Wendy, Huang

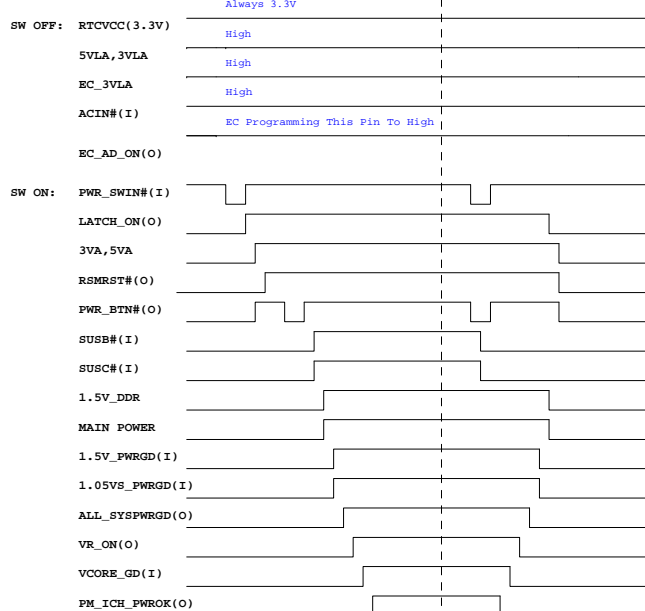
Power on/off sequence AC insert (without Battery Pack)

Power on sequence Power off sequence



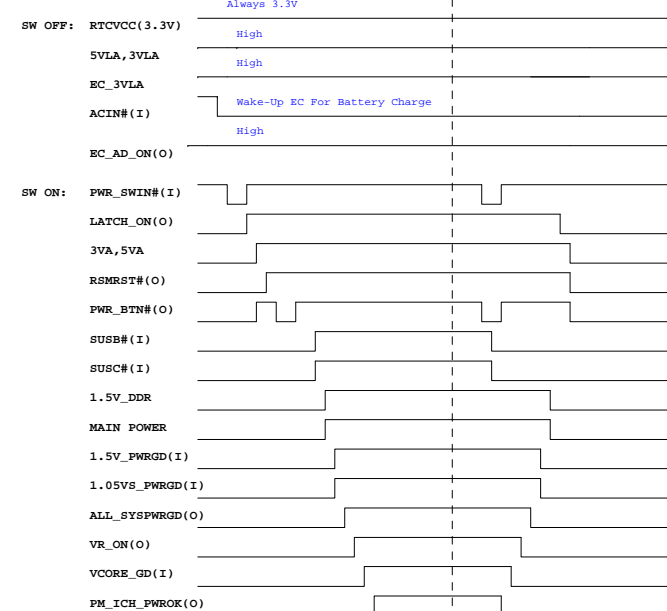
Power on/off sequence Battery insert (without AC adapter)

Power on sequence Power off sequence



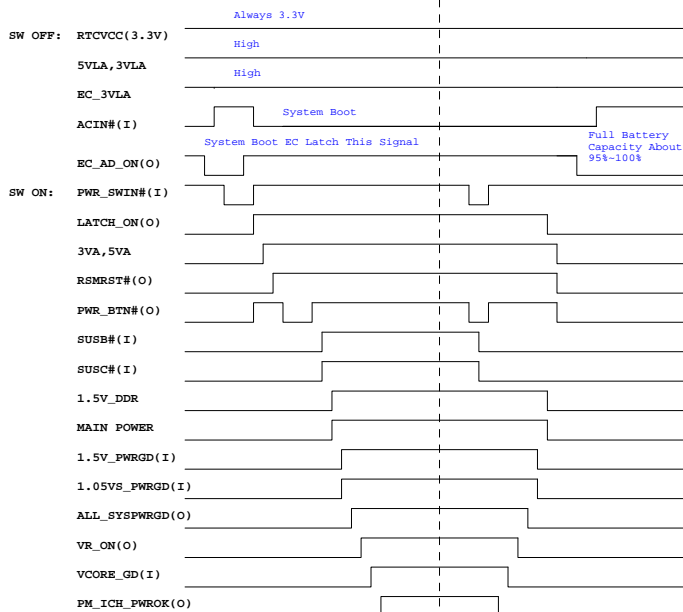
Power on/off sequence AC insert(with charge over 95%)

Power on sequence Power off sequence



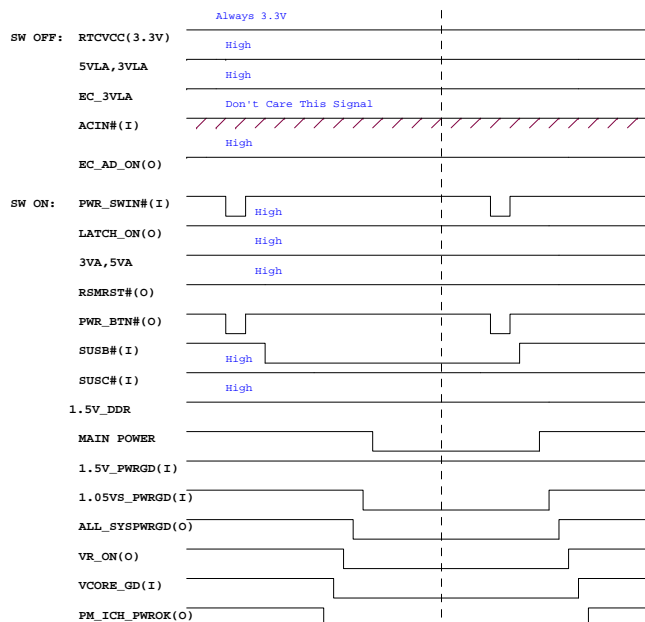
Power on/off sequence AC insert(without charge over 95%)

Power on sequence Power off sequence



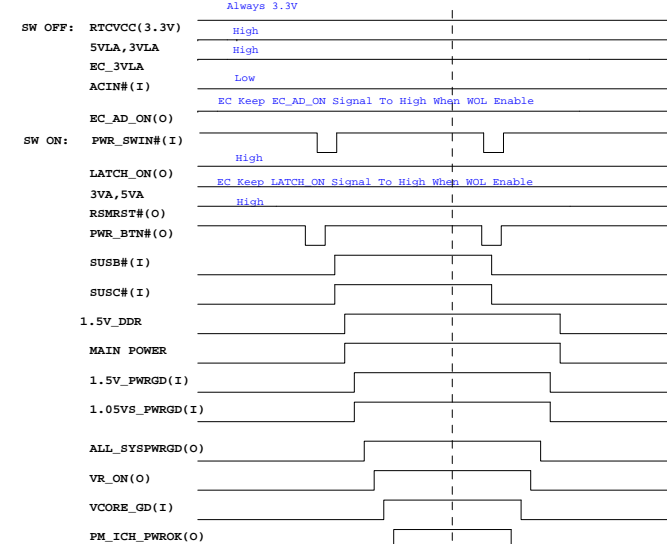
Suspend And Resume Sequence (S3)

Suspend sequence Resume sequence



Power on/off sequence after windows shutdown (WOL enable)

Suspend sequence Resume sequence



INVENTEC

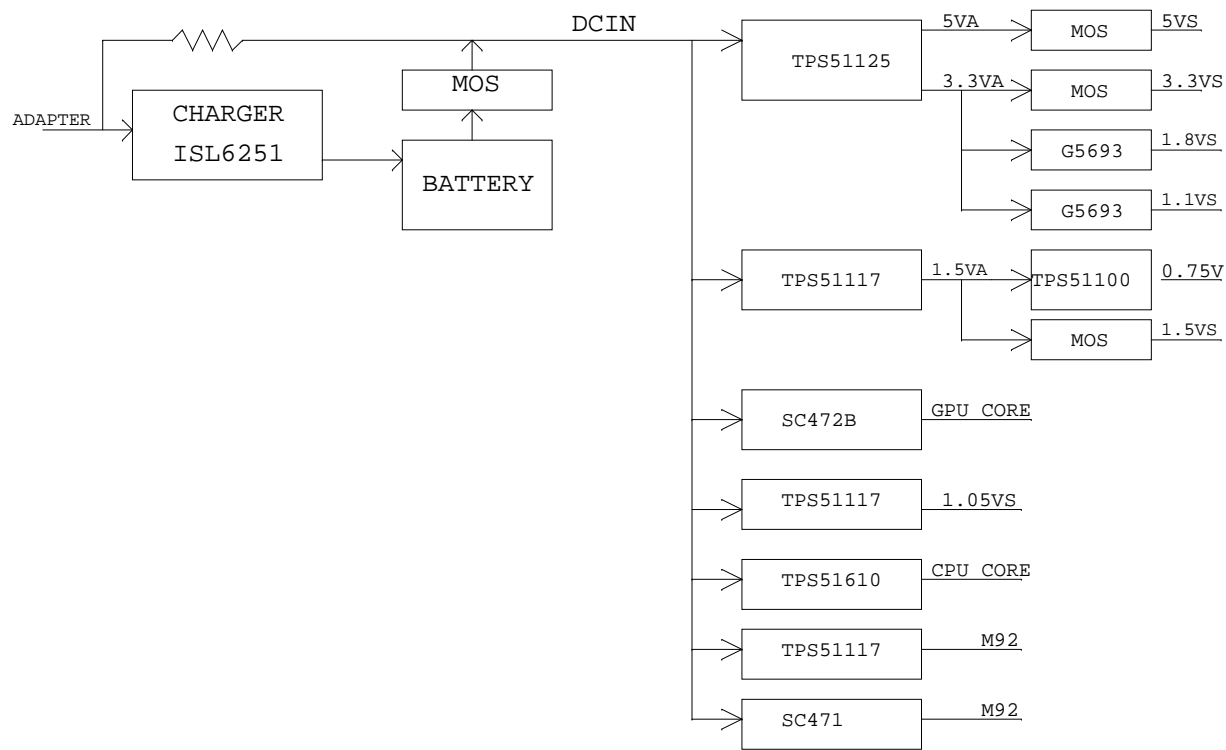
MODEL
BAP41/BAP51 (Montevina SFF)
Title Diagram

SIZE CODE
Custom A02
DOC NUMBER
D-CS-1310A2282001-ALG
REV
A02

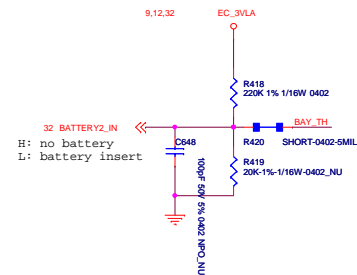
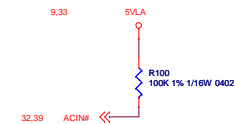
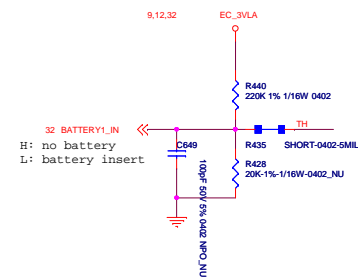
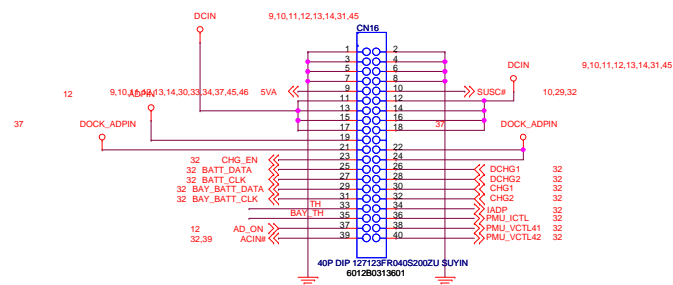
CHANGE by Shun-Chin Chen DATE Monday, June 29, 2009

SHEET 6 of 49

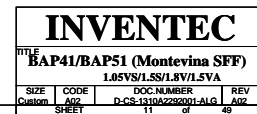
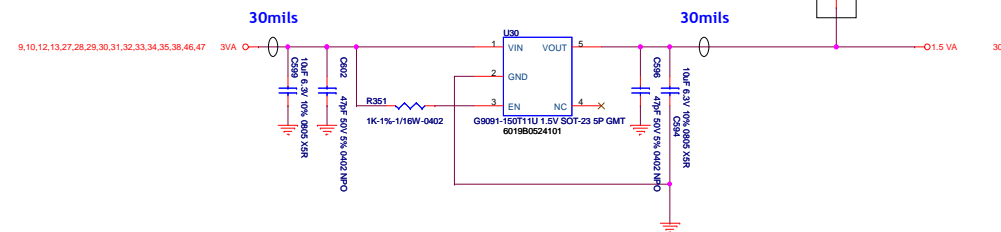
Power Block Diagram :



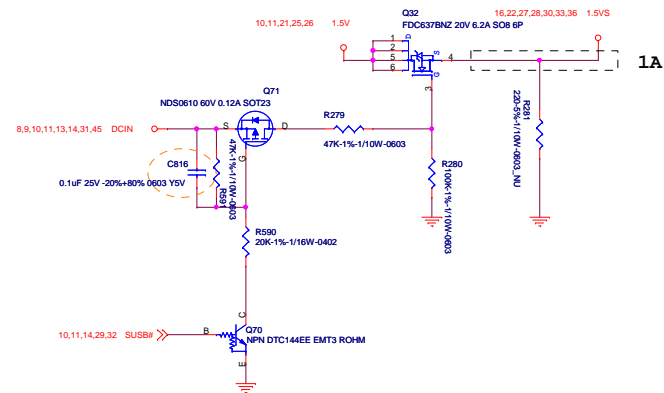
Charger CN TO USIM/B



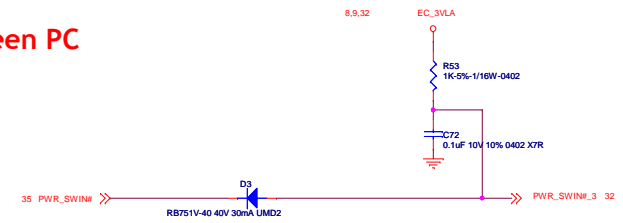
INVENTEC				
TITLE BAP41/BAP51 (Montevina SFF)				
Adaptor In / Charge				
SIZE	CODE	DOC NUMBER	REV	
Custom	AP2	D-CS-1310A220001-ALG	A02	
CHANGE by Shun-Chin Chang			DATE	Wednesday, July 01, 2009
SHEET			8	of 49



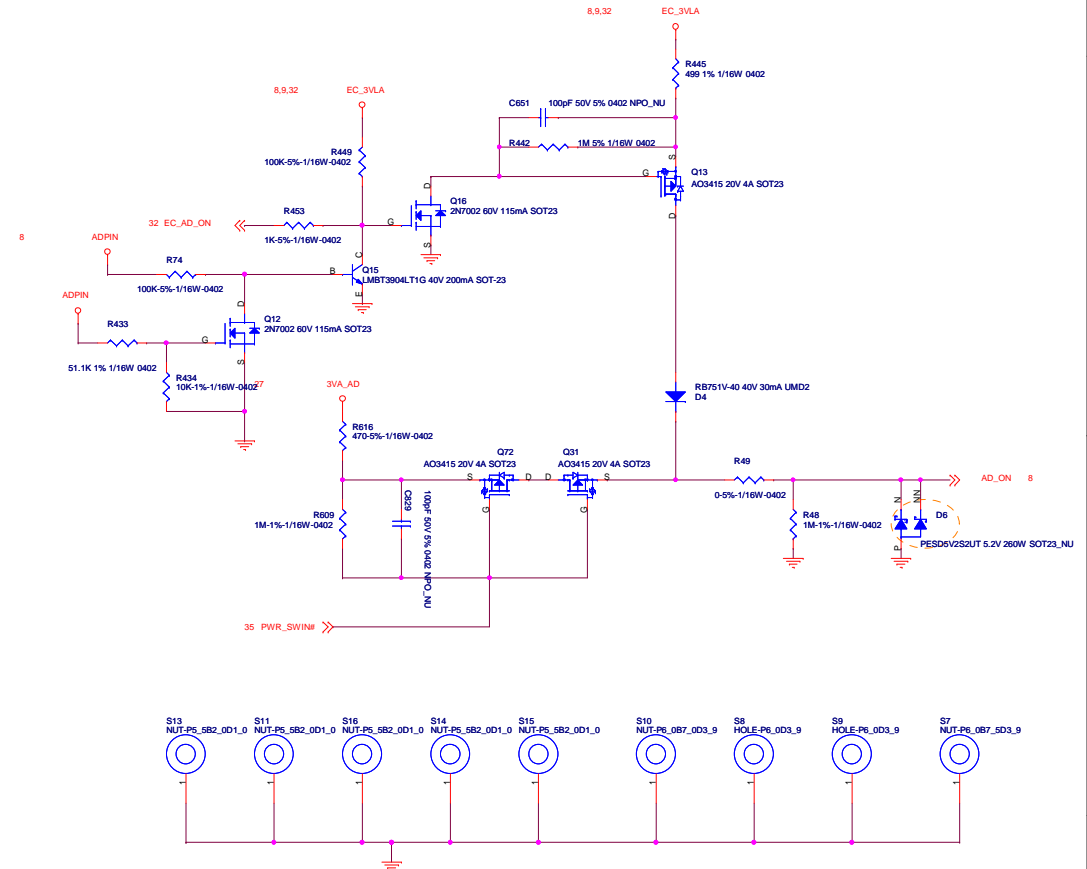
1.5VS



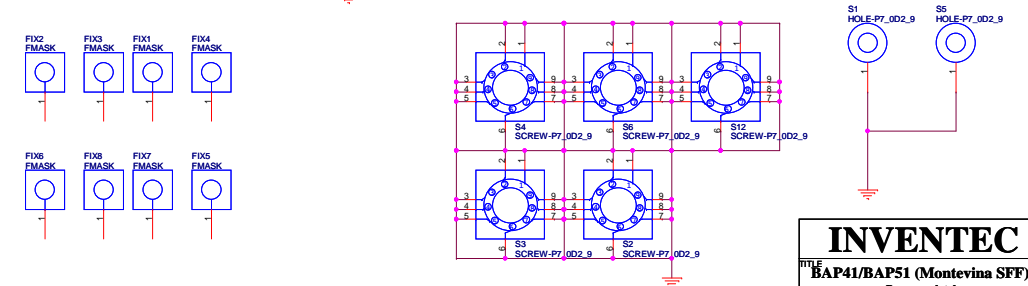
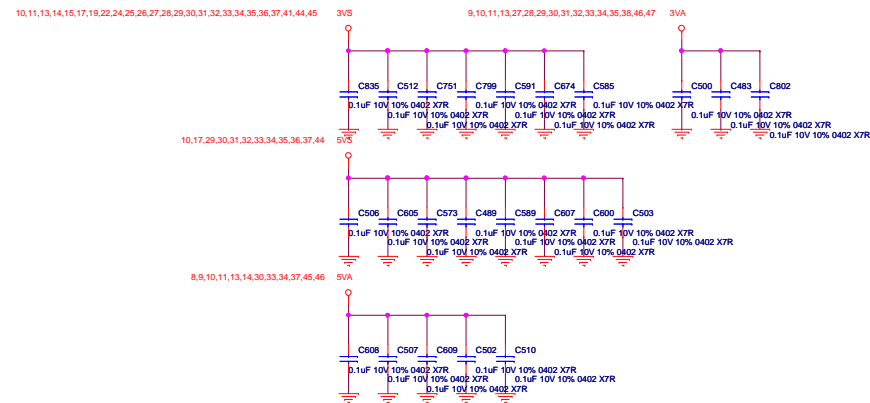
For Green PC



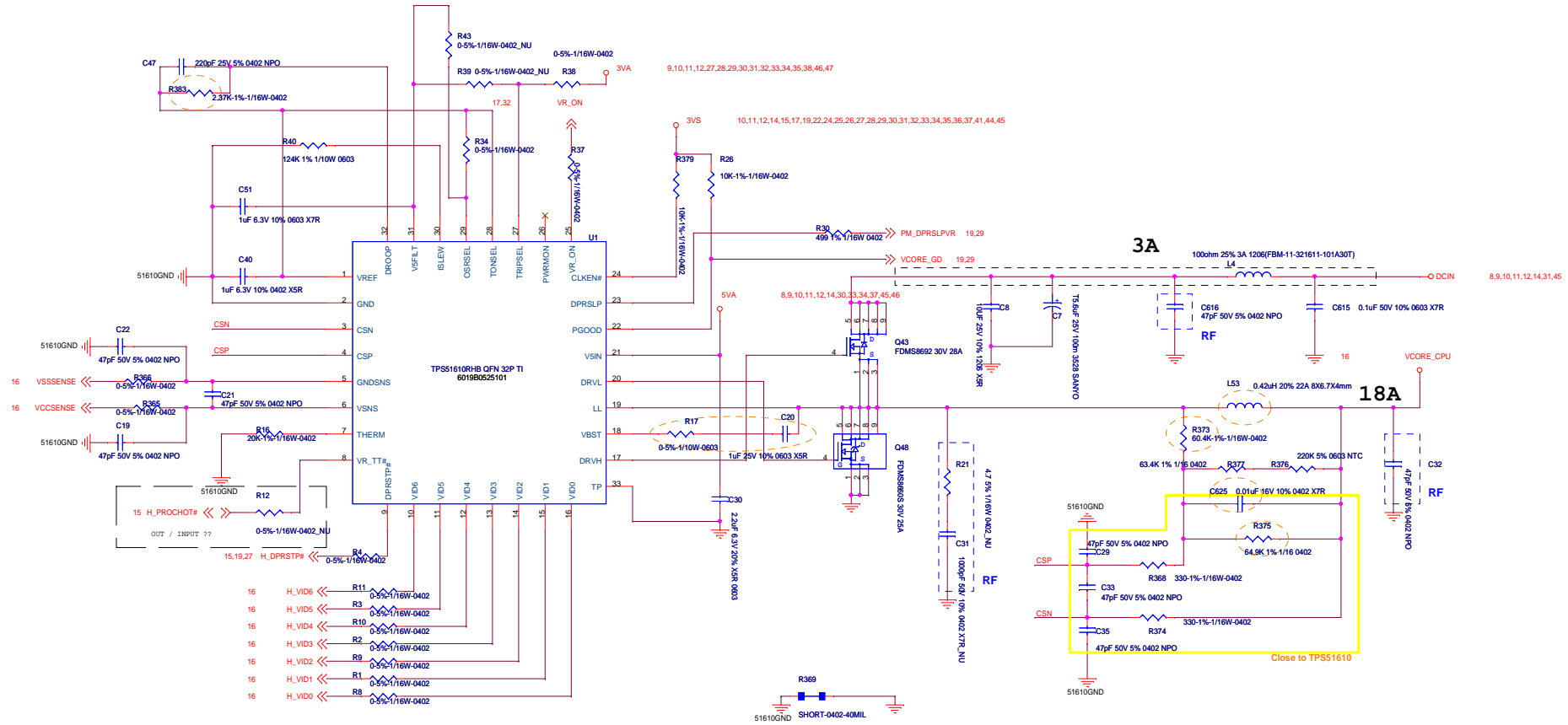
None Green PC ---- NU

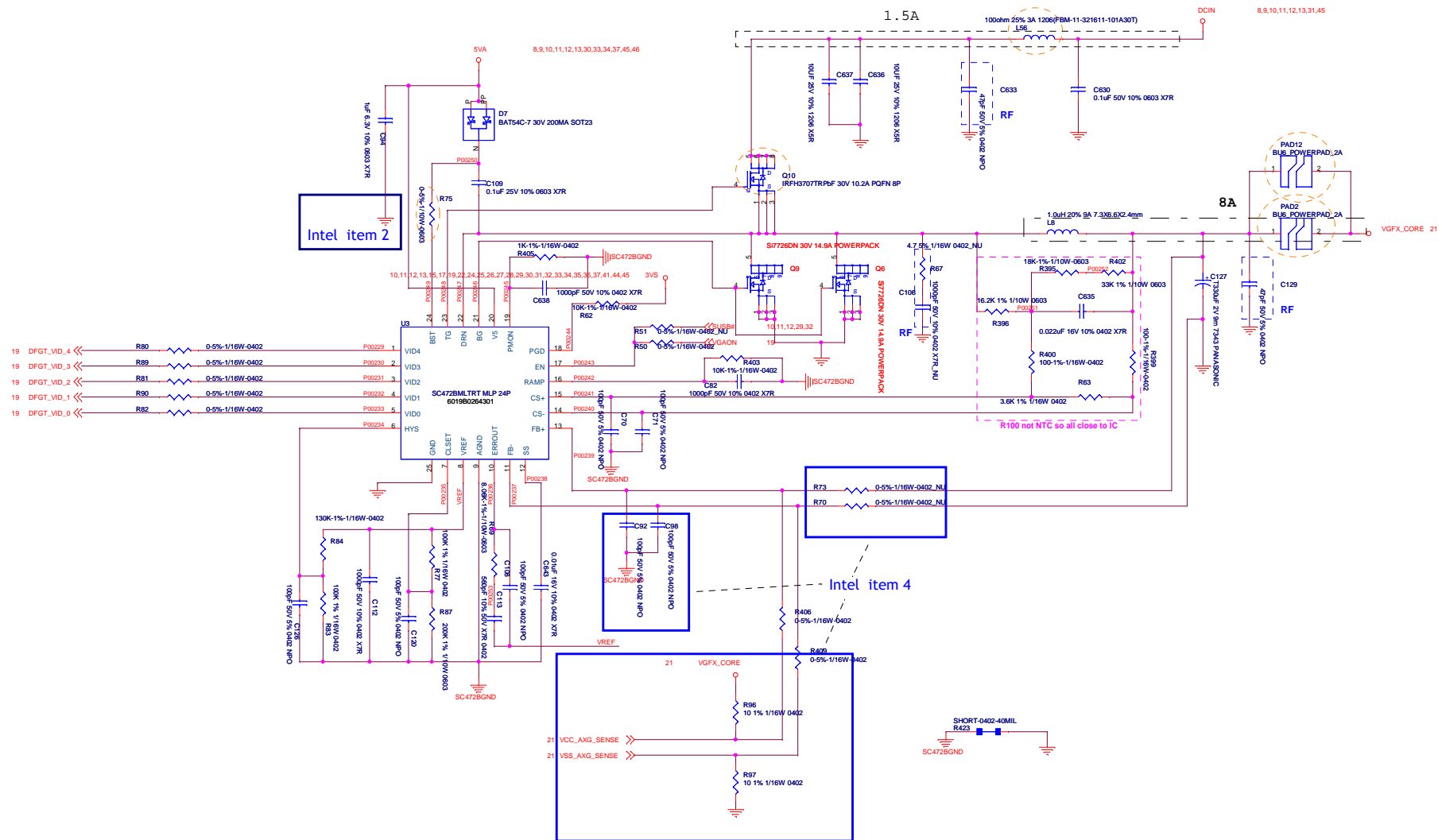


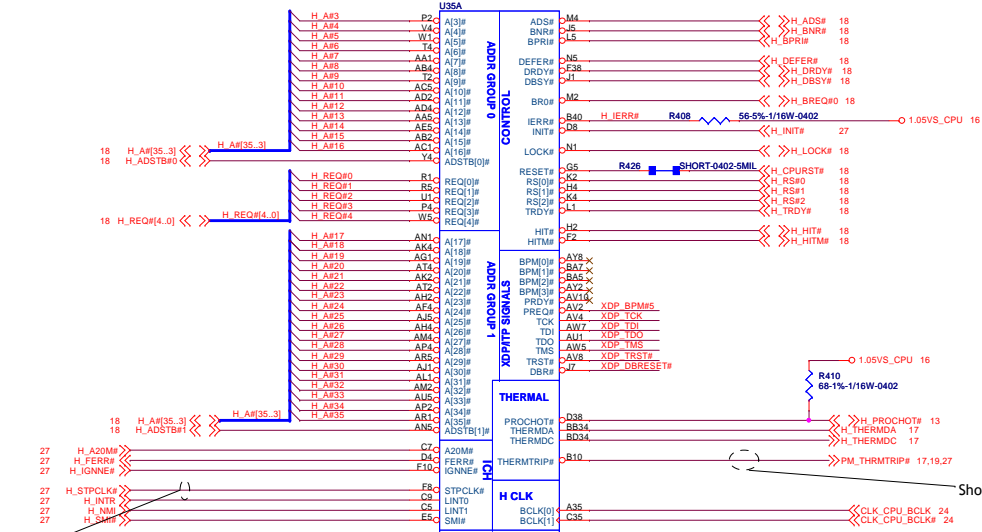
EMI Cap



INVENTEC			
TITLE BAP41/BAP51 (Montevina SFF)			
Power on latch			
SIZE Custom	CODE A02	DOC. NUMBER D-CS-1310A2292001-ALG	REV A02
SHEET		12 of	49

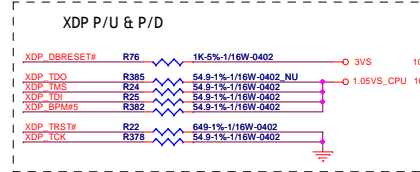




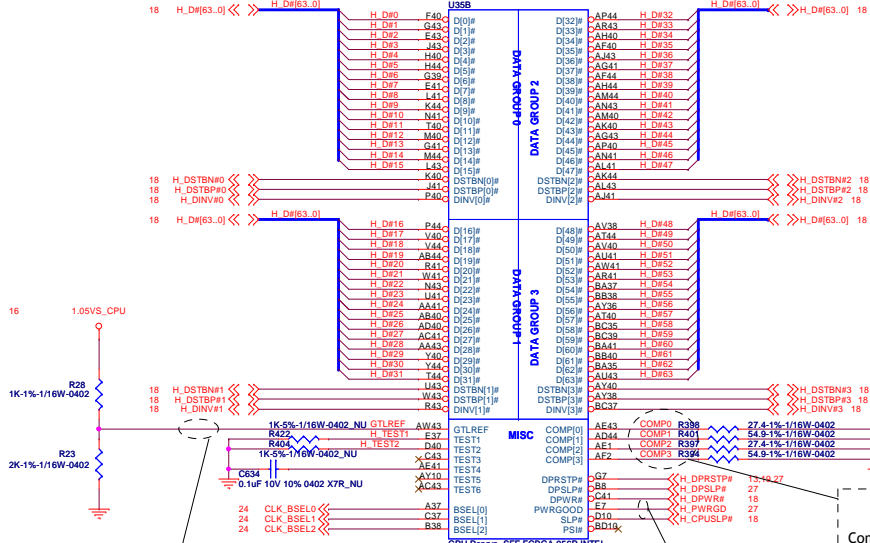


No stub on H_STPCLK test point

Route to TP via and place gnd via w/in 100mils



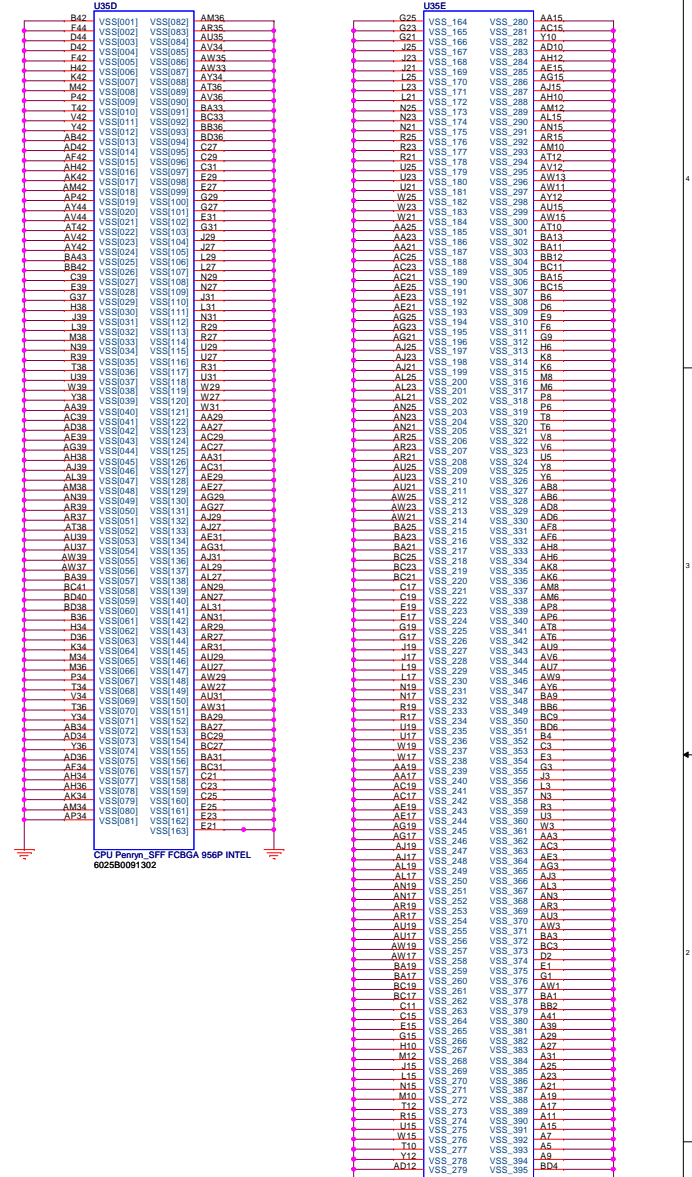
A#[32-39], APM#[0-1]: Leave escape routing on for future functionality



Zo=55ohm, 0.5" max for GTLREF, Space any other switch signals away from GTLREF with a minimum of 25mils. Don't allow the GTLREF routing to create splits or discontinuities in the reference planes of the FSB signals

H_PWRGD rise time : Max : 15ns

Comp0,2 connect with Zo=27.4ohm, make trace length shorter than 0.5" and width is 18mils. Comp1,3 connect with Zo=55ohm, make trace length shorter than 0.5" and width is 5mils

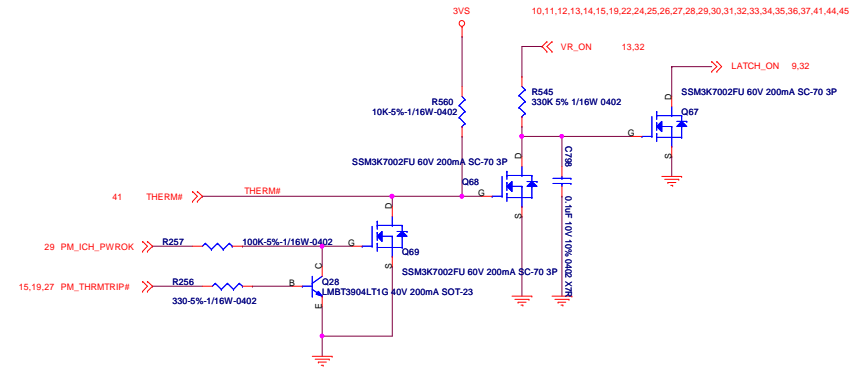
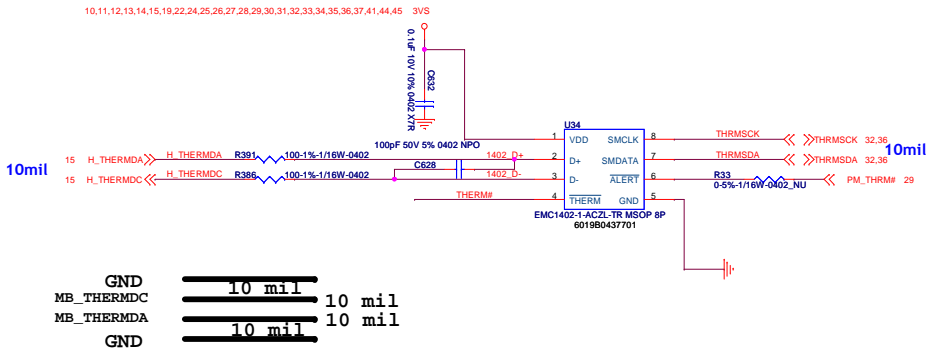


CPU Pin 101 to 200

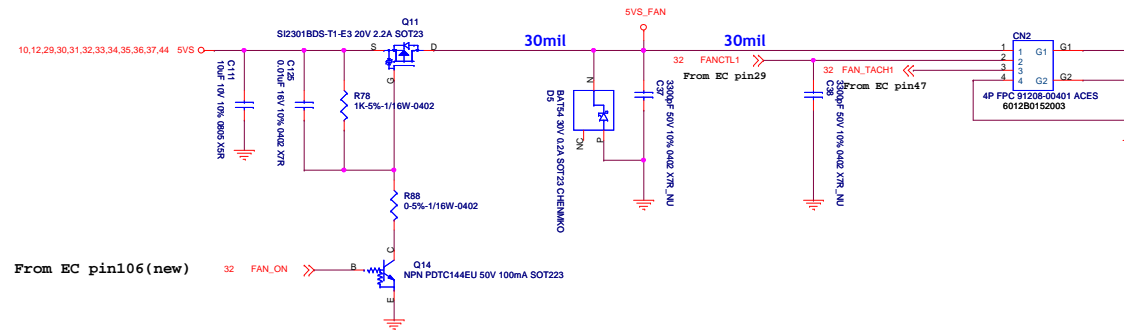
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Custom	A02	D-C-1310A222001	A02
SHEET	15		



THERMAL SENSOR



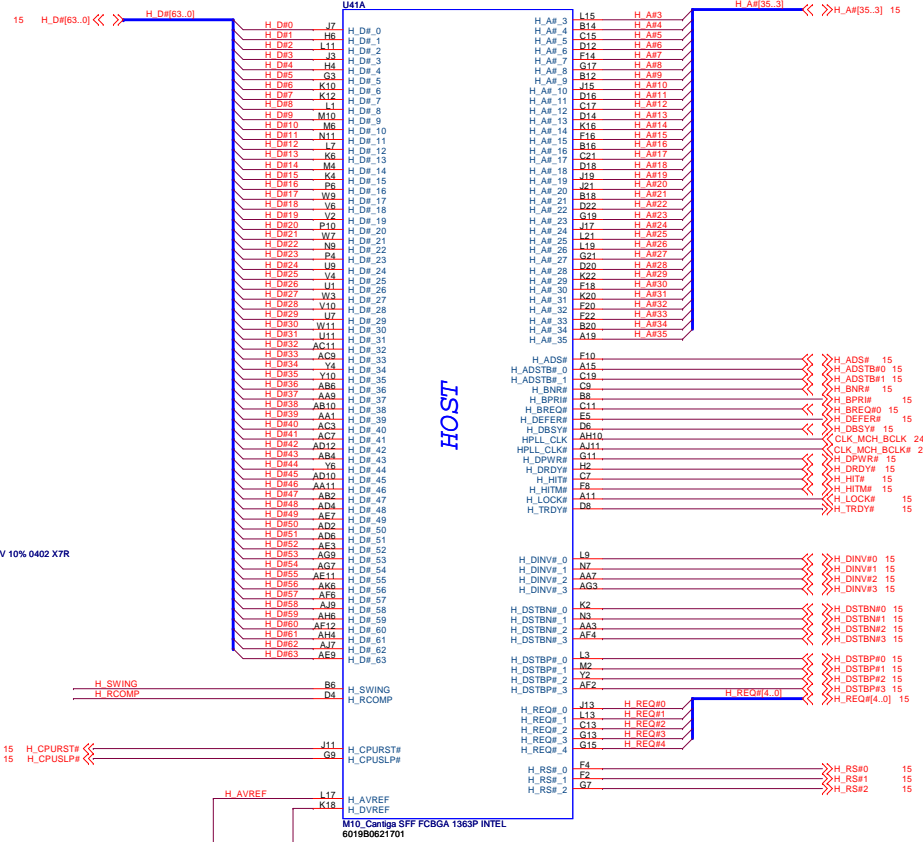
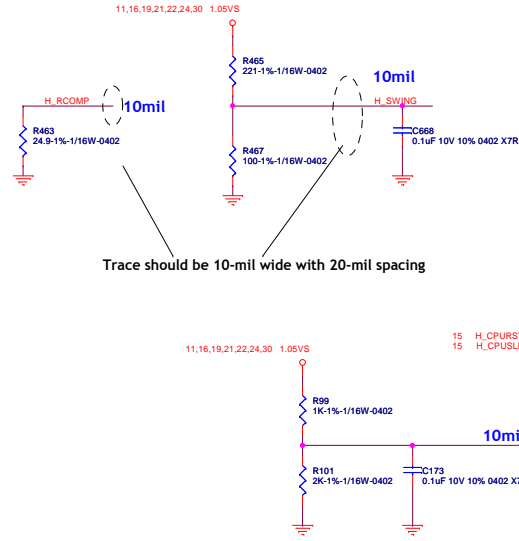
Fan control

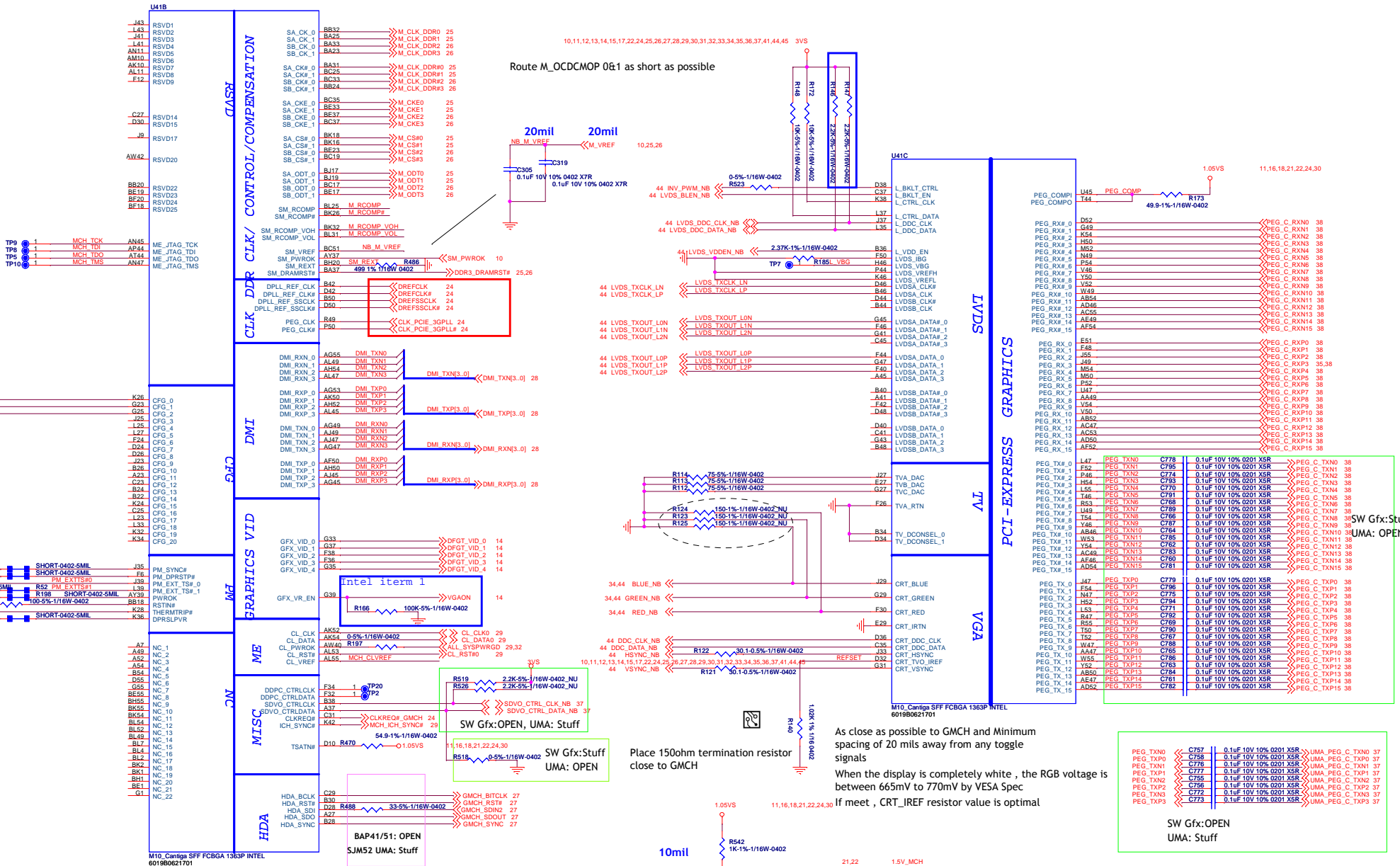
**INVENTEC**

BAP41/BAP51 (Montevina SFF)

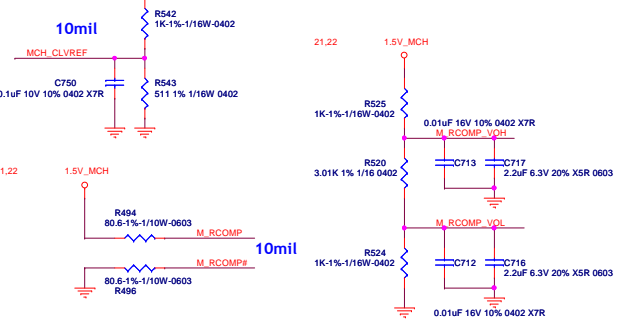
CPU Thermal

SIZE Custom	CODE A02	DOC. NUMBER D-CS-1310A2292001-ALG	REV A02
SHEET		17 of	49





Cantiga Strapping:		
	Low	High
MCH_CFG5	DMIx2	DMIx4
MCH_CFG6(I7PM Host I/F)	Enable	Disable(default)
MCH_CFG7(TLS confidentiality)	With	With no(default)
MCH_CFG9 (PCIe Graphic Lane)	Reverse Lane	Normal Operation
MCH_CFG10 (PCIe loopback)	Enable	Disable(default)
MCH_CFG12 (ALL2)	Enable	Disable(default)
MCH_CFG13(XOR)	Enable	Disable(default)
MCH_CFG16 (FSB Dynamic ODT)	Dynamic ODT Disable	Dynamic ODT Enable
MCH_CFG19 (DMI Lane Reversal)	Normal	Lanes Reversed
MCH_CFG20	Only (SDVO/DP/HD) or PCIe is operational	SDVO/DP/HD and PCIe are operating simultaneously via the PEG port



DISPLAY OUT STRAPPING		
	LOW	HIGH
SDVO_CTRLDATA	SDVO/IHD/DP disabled (default)	SDVO/IHD/DP enabled
L_DDC_DATA	LFP disabled (default)	LFP Card Present: PCIe disabled
DDPC_CTRLDATA	Digital display (iHD/DP) disabled (default)	Digital display (iHD/DP) enabled

INVENTEC

TITLE

BAP41/BAP51 (Montevina SFF)

SIZE

A02

CODE

D-CB-1104228001-ALG

SHEET

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DATE

Wednesday, July 01, 2009

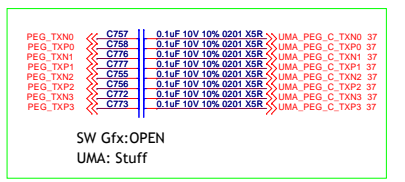
CHANGE by

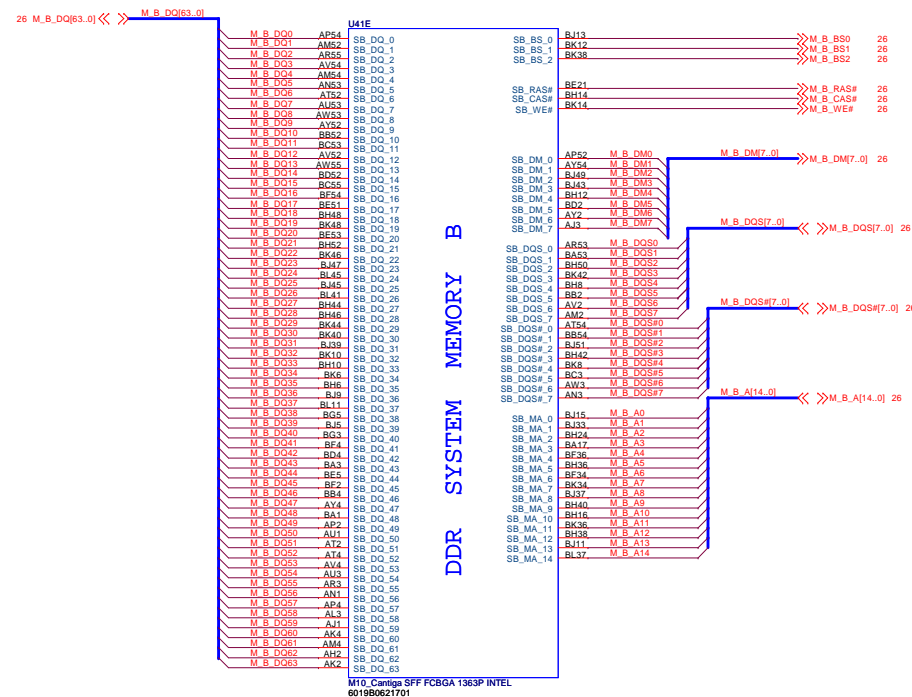
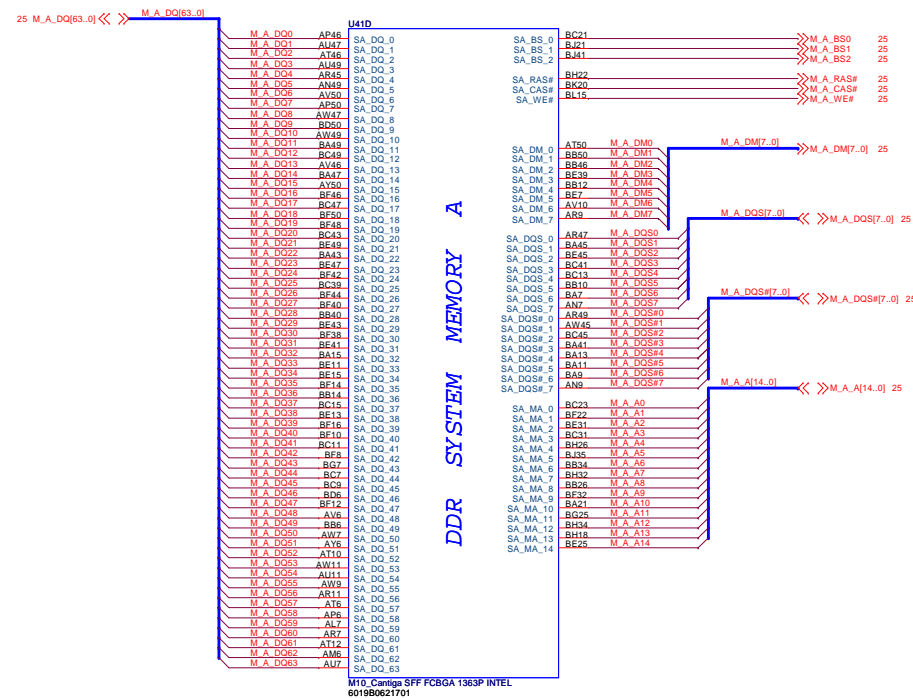
Shun-Chin Chan

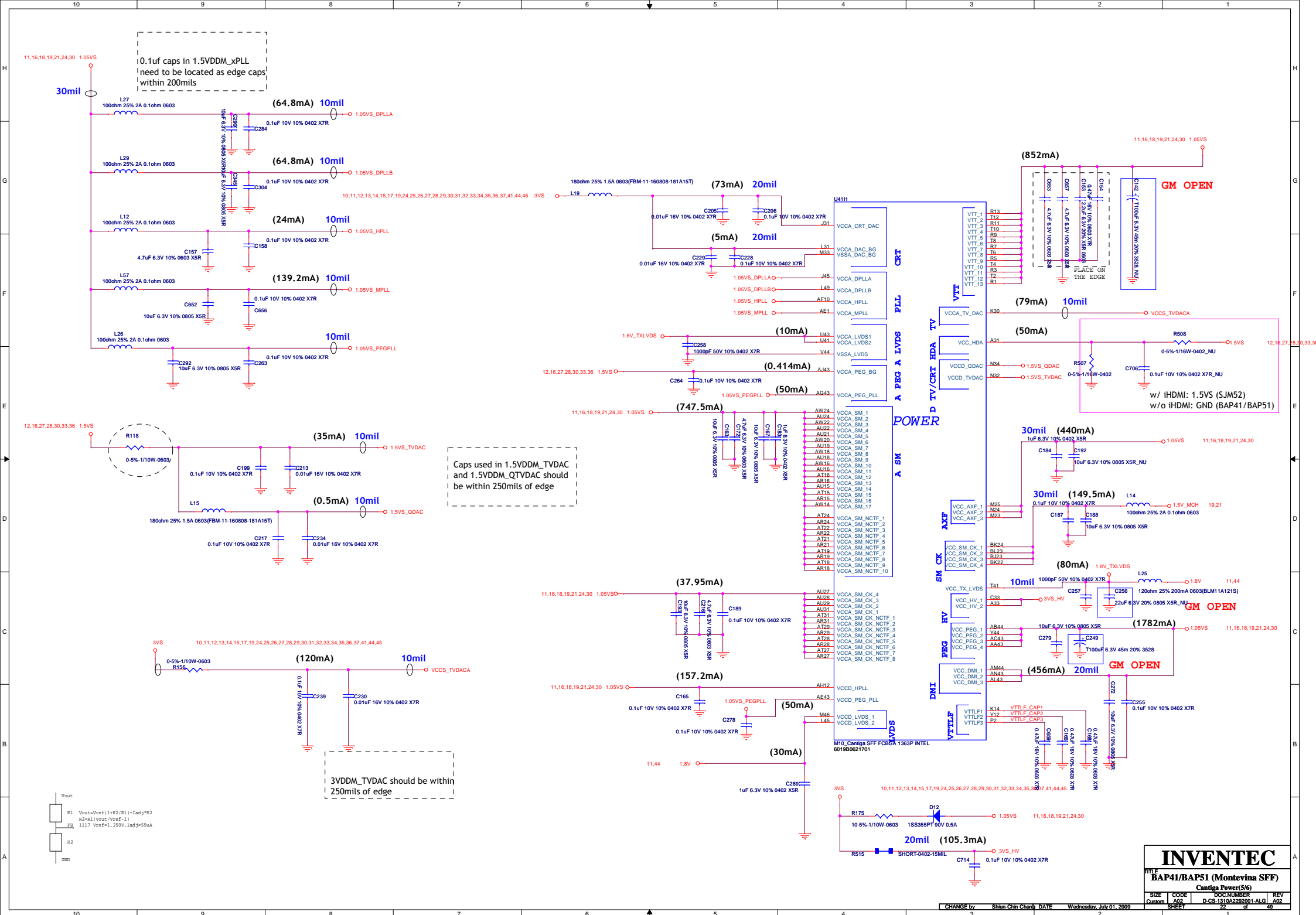
As close as possible to GMCH and Minimum spacing of 20 mils away from any toggle signals

When the display is completely white , the RGB voltage is between 665mV to 770mV by VESA Spec

If meet , CRT_IREF resistor value is optimal



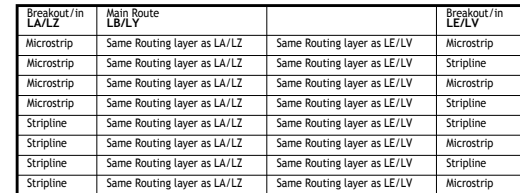




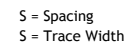

```

graph LR
    subgraph SMCH
        Tx1[Tx] --> LA1[LA1]
        LA1 --> LA2[LA2]
        LA2 --> LB[LB]
        LB --> LC[LC]
        LC --> LD[LD]
        LD --> LE[LE]
        LE --> ICH8mRx[ICH8m Rx]
        
        Rx1[Rx] --> LZ1[LZ1]
        LZ1 --> LZ2[LZ2]
        LZ2 --> LY[LY]
        LY --> LX[LX]
        LX --> LW[LW]
        LW --> LV[LV]
        LV --> ICH8mTx[ICH8m Tx]
    end
    subgraph ICH8m
        ICH8mRx
        ICH8mTx
    end

```

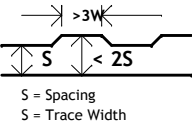
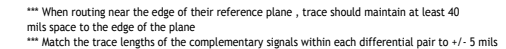


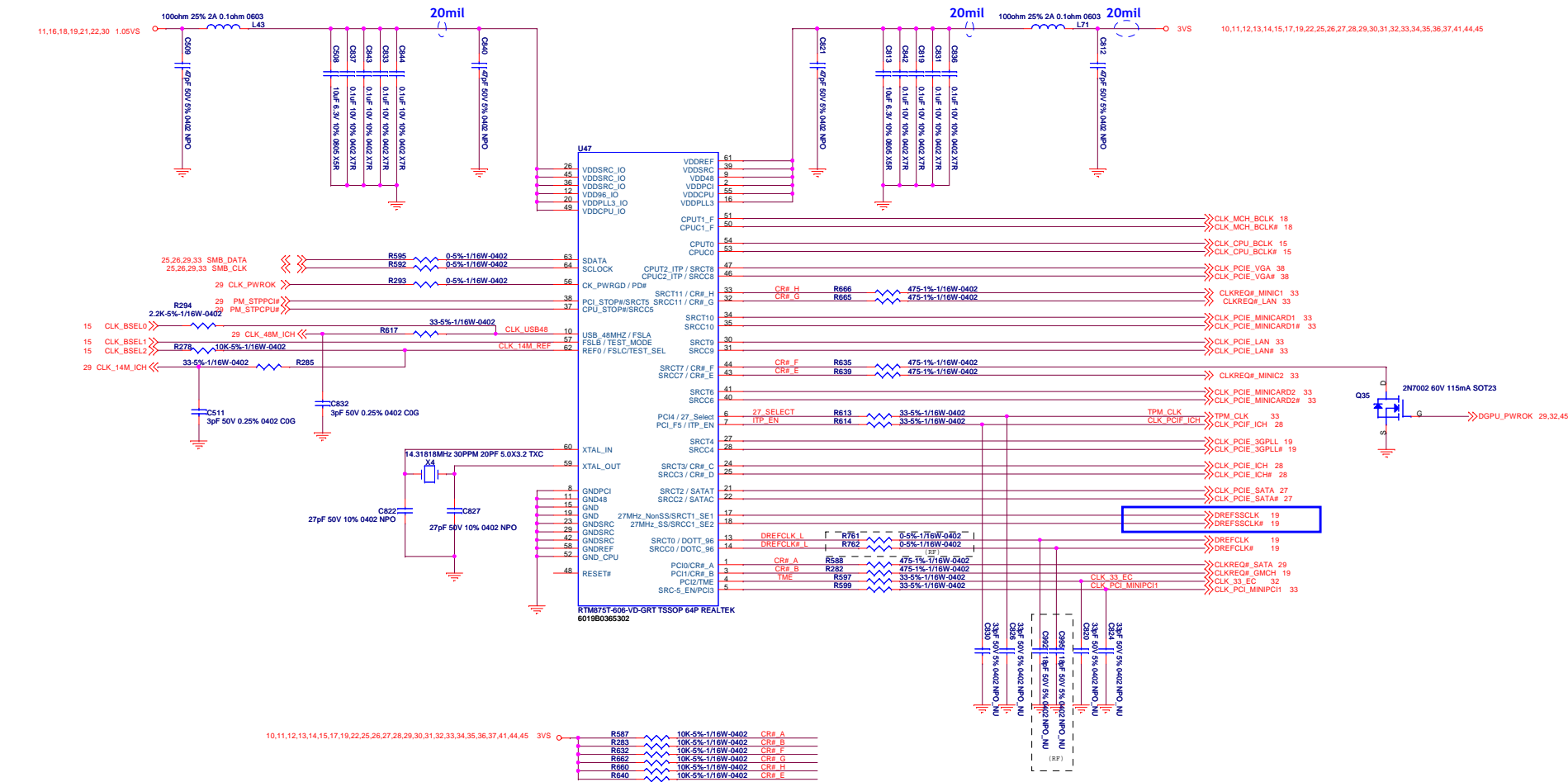
*** Match the trace lengths of the complementary signals within each differential pair to ± 5 mils



```

graph LR
    subgraph GMCH
        Tx1[Tx]
        Rx1[Rx]
    end
    subgraph ExpressMiniCard [Express/Mini Card]
        Rx2[Rx]
        Tx2[Tx]
    end
    Tx1 --- LA --- LB --- LC --- Rx2
    Rx1 --- LZ --- LY --- Tx2
    style LA fill:none,stroke:none
    style LB fill:none,stroke:none
    style LC fill:none,stroke:none
    style LZ fill:none,stroke:none
    style LY fill:none,stroke:none
    
```





15 CLK_BSEL2 >> R275 >> 1K5%-1/16W-0402 >> MCH_BSEL2 19
15 CLK_BSEL1 >> R291 >> 1K5%-1/16W-0402 >> MCH_BSEL1 19
15 CLK_BSEL0 >> R287 >> 1K5%-1/16W-0402 >> MCH_BSEL0 19

FSA	FSE	FSC	FSE	CLOCK FREQUENCY	HOST CLOCK FREQUENCY
1	1	0	667	166	
0	1	0	800	200	
0	0	0	1067	266	*

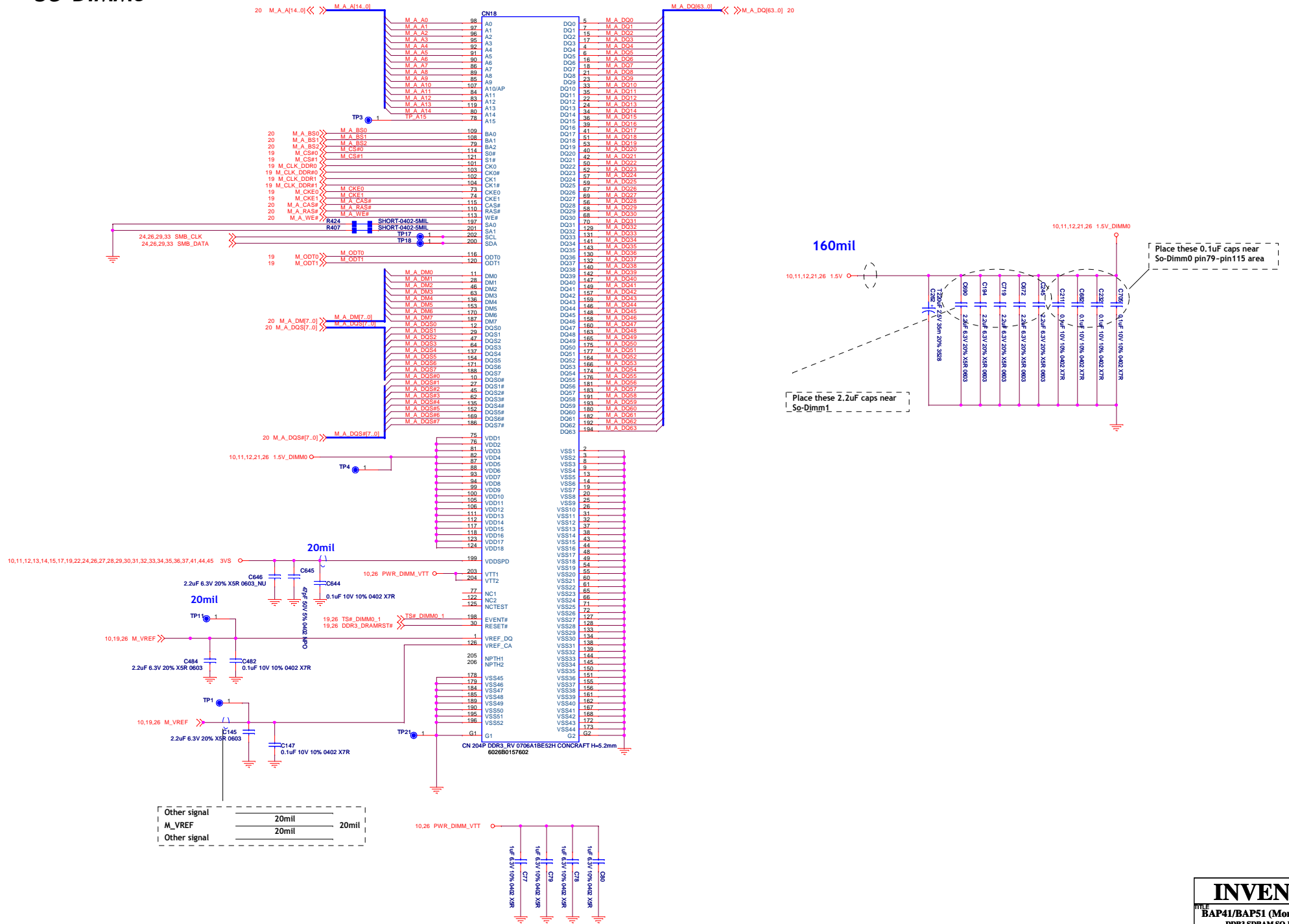
ITP_EN = 0
SRC6 / SRC8#
ITP_EN = 1
ITP / ITP#

27_SELECT = 0
Dot96 / LCD_SS / SE
27_SELECT = 1
SRC0 / 27Hz

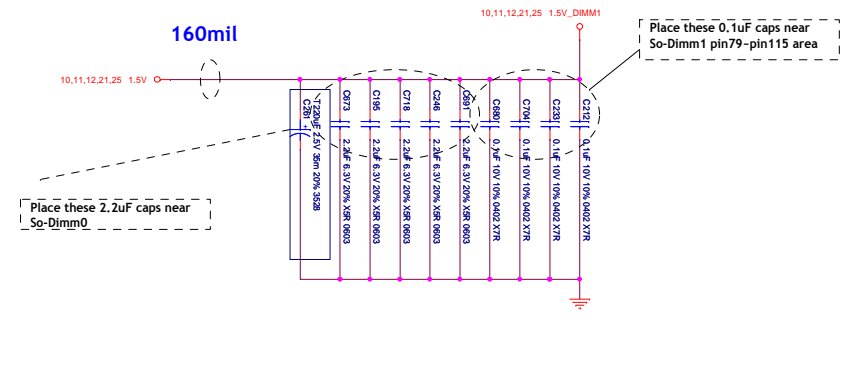
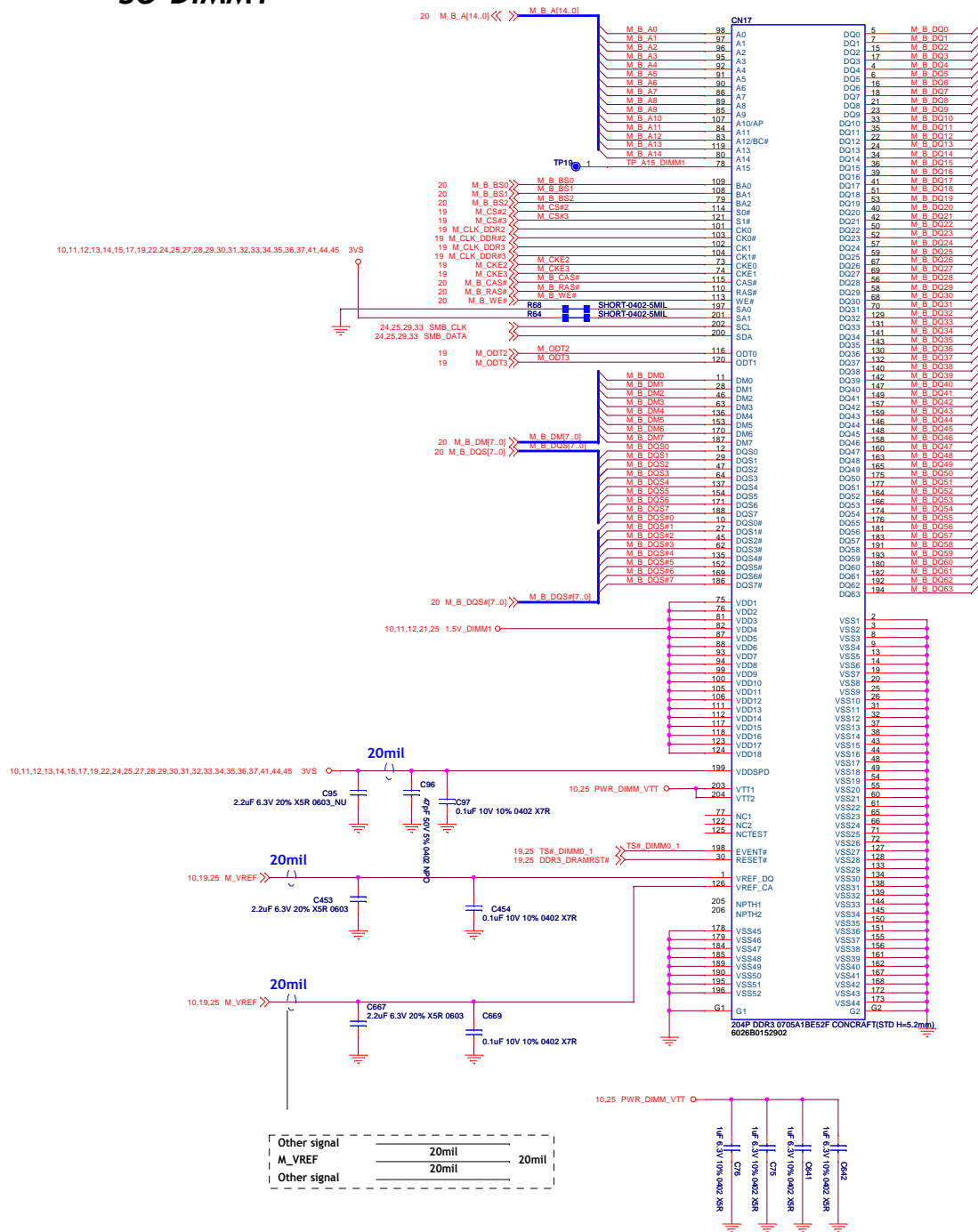
3V3
R284 10K5%-1/16W-0402
R286 10K5%-1/16W-0402_NU

CR#_A:	Byte 5 bit 6=0---->SRC0 bit 6=1---->SRC2	BIT 7=1 (Enable)
CR#_C:	Byte 5 bit 2=0---->SRC0 bit 2=1---->SRC2	BIT 3=1 (Enable)
CR#_B:	Byte 5 bit 4=0---->SRC1 bit 4=1---->SRC4	BIT 5=1 (Enable)
CR#_D:	Byte 5 bit 0=0---->SRC1 bit 0=1---->SRC4	BIT 1=1 (Enable)
CR#_E:	SRC6 (Byte 6)	BIT 7=1 (Enable)
CR#_F:	SRC8 (Byte 6)	BIT 6=1 (Enable)
CR#_G:	SRC9 (Byte 6)	BIT 5=1 (Enable)
CR#_H:	SRC10 (Byte 6)	BIT 4=1 (Enable)

SO-DIMMO



SO-DIMM 1

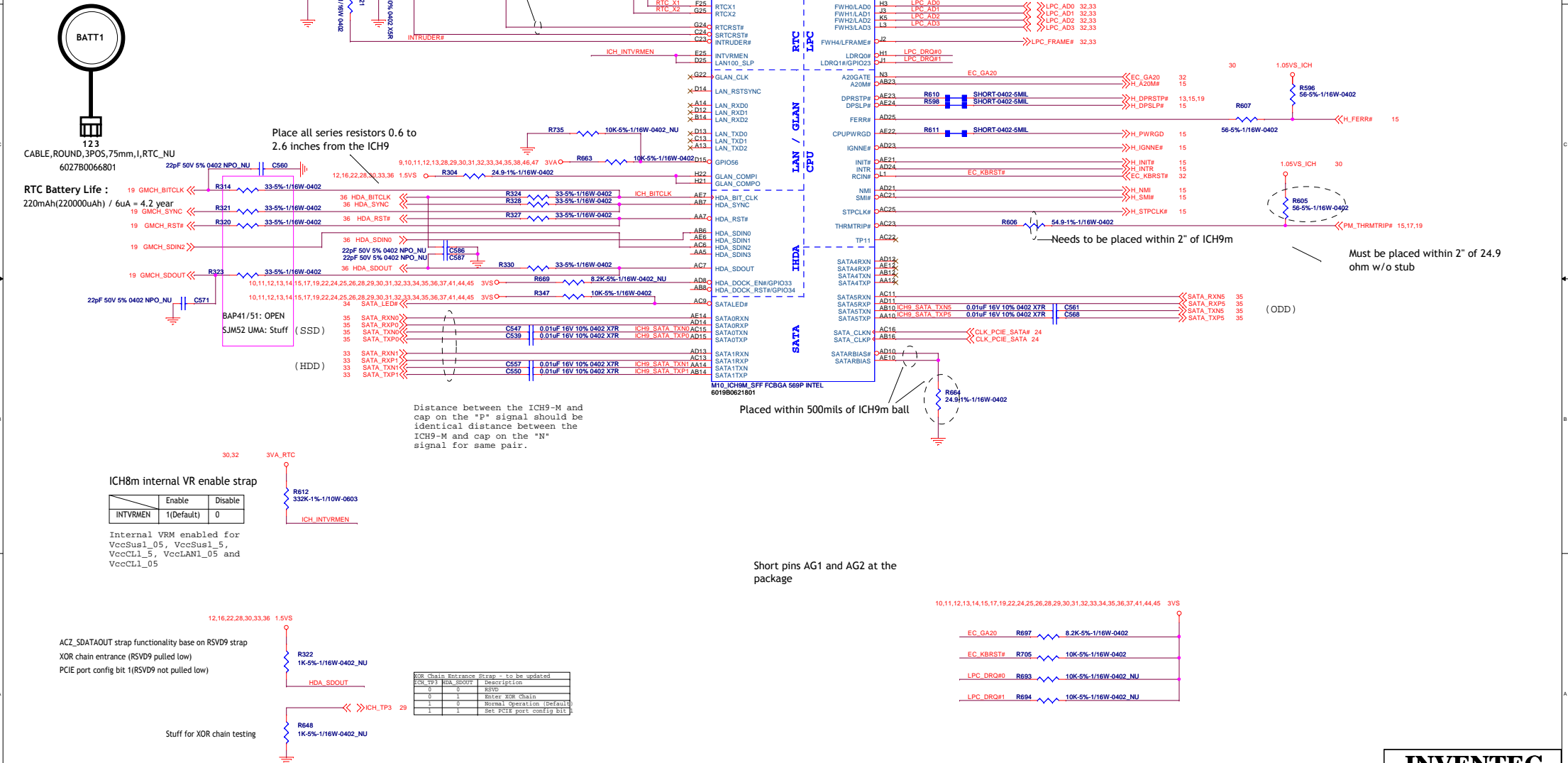


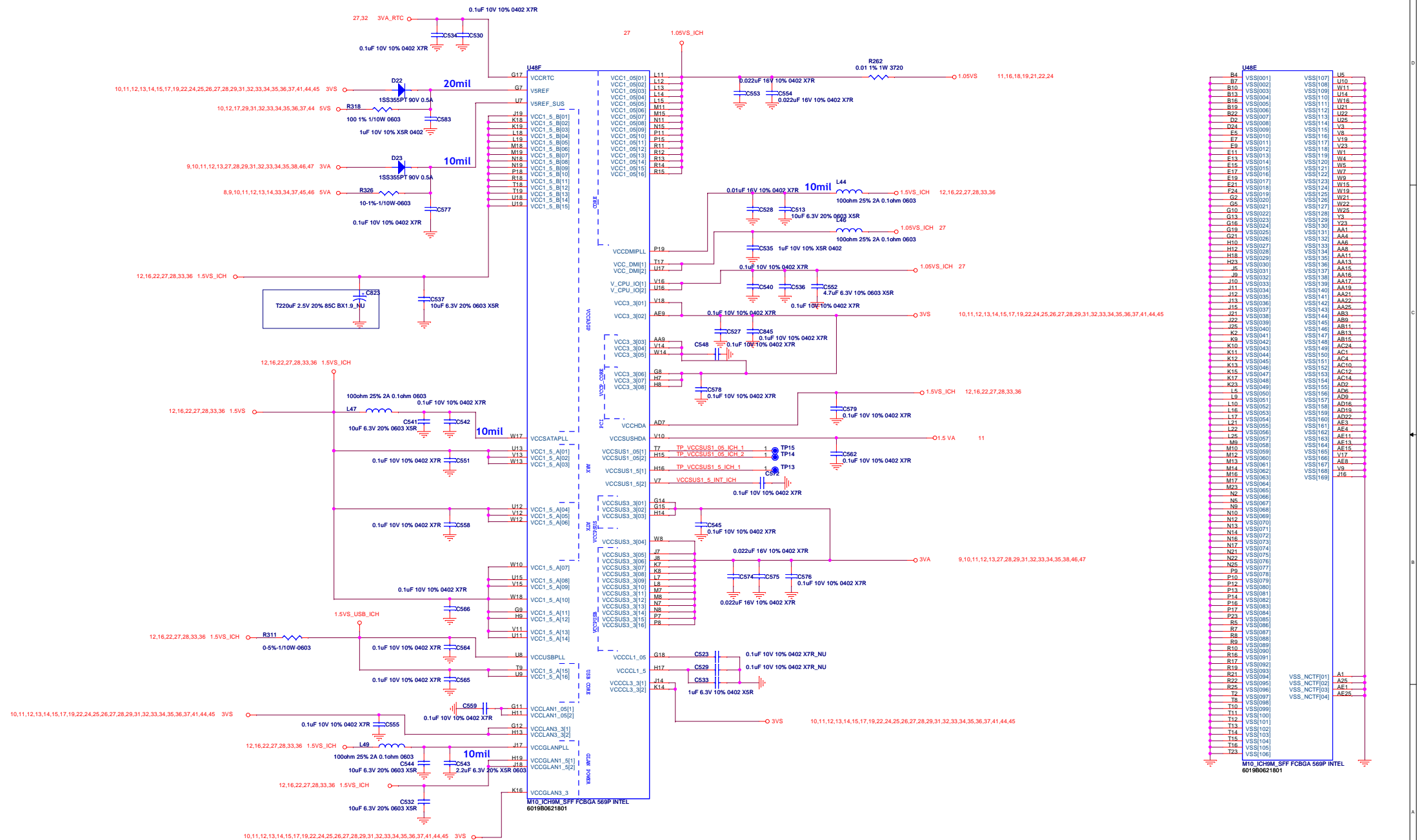
RTC Circuit

1. RC delay time should be in the range of 18-25ms
2. It is recommended that this larger capacitor and small resistor value in order to reduce the likelihood of glitching of RTCRST#

1. The ICH7m requires a length less than 1 inch on each branch (from crystal's terminal to RTCXn ball)
2. Routing the RTC circuit should be kept simple to simplify the trace length measurement and increase accuracy on calculating trace capacitances
3. On FR-4, a 5-mils trace has approximately 2pF per inch
4. Trace signal coupling must limited as much as possible by avoiding the routing of adjacent PCI signals close to RTCX1 and RTCX2
5. Ground guard plane is highly recommended

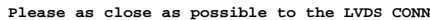
For Green PC





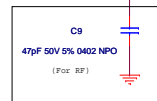
U48E	VSS[001]	U6
B4	VSS[002]	U10
B10	VSS[003]	U11
B11	VSS[004]	U12
B12	VSS[005]	U13
B13	VSS[006]	U14
B14	VSS[007]	U15
B15	VSS[008]	U16
B16	VSS[009]	U17
B17	VSS[010]	U18
B18	VSS[011]	U19
B19	VSS[012]	U20
B20	VSS[013]	U21
B21	VSS[014]	U22
B22	VSS[015]	U23
B23	VSS[016]	U24
B24	VSS[017]	U25
B25	VSS[018]	U26
B26	VSS[019]	U27
B27	VSS[020]	U28
B28	VSS[021]	U29
B29	VSS[022]	U30
B30	VSS[023]	U31
B31	VSS[024]	U32
B32	VSS[025]	U33
B33	VSS[026]	U34
B34	VSS[027]	U35
B35	VSS[028]	U36
B36	VSS[029]	U37
B37	VSS[030]	U38
B38	VSS[031]	U39
B39	VSS[032]	U40
B40	VSS[033]	U41
B41	VSS[034]	U42
B42	VSS[035]	U43
B43	VSS[036]	U44
B44	VSS[037]	U45
B45	VSS[038]	U46
B46	VSS[039]	U47
B47	VSS[040]	U48
B48	VSS[041]	U49
B49	VSS[042]	U50
B50	VSS[043]	U51
B51	VSS[044]	U52
B52	VSS[045]	U53
B53	VSS[046]	U54
B54	VSS[047]	U55
B55	VSS[048]	U56
B56	VSS[049]	U57
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B58	VSS[051]	U59
B59	VSS[052]	U60
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B		

Q64
TPC6104 20V 5 5A SSOT 6P



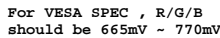
LCD brightness control

WEB Cam.



CRT

No stub



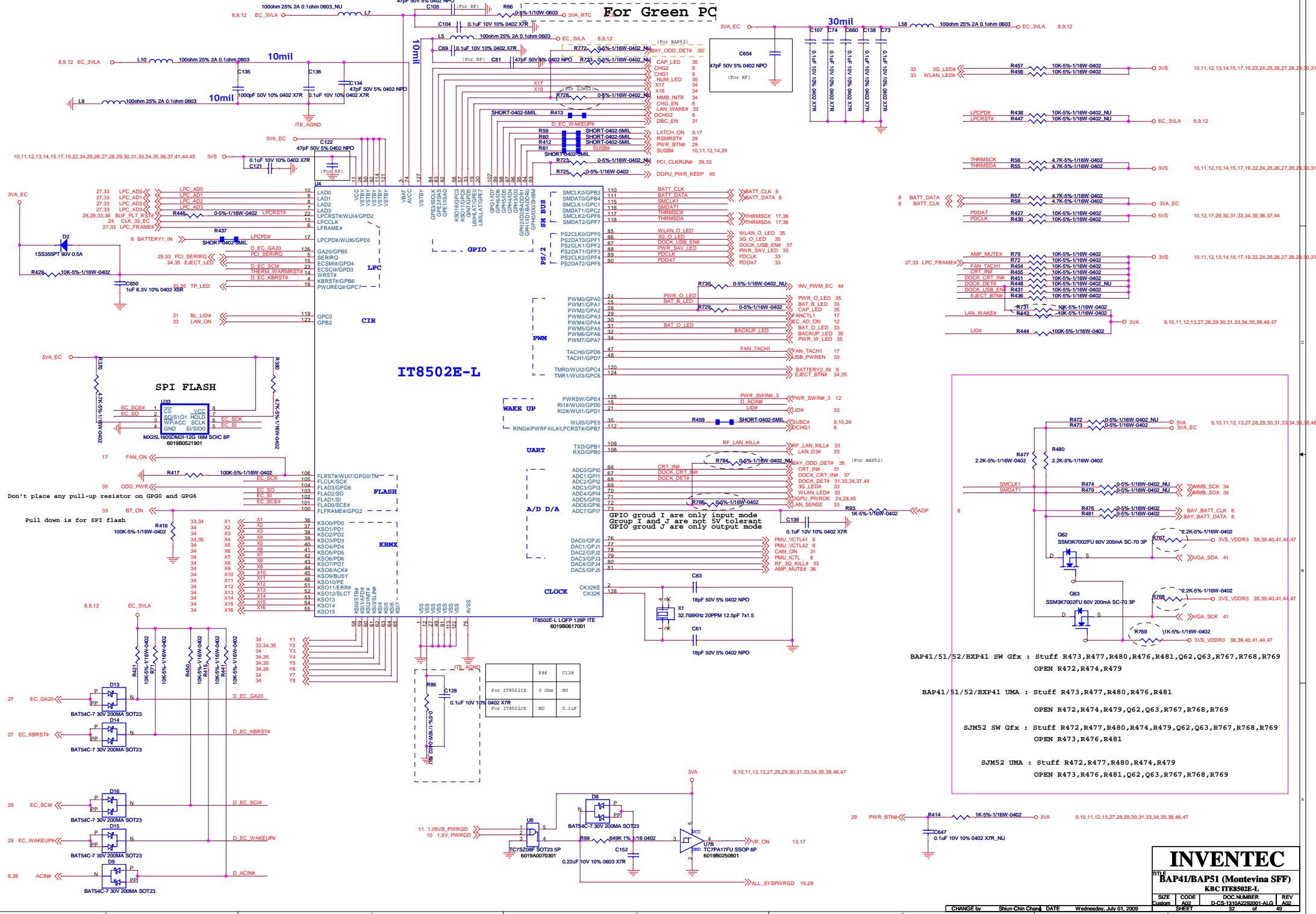
Change to 47p for VESA

INVENTEC

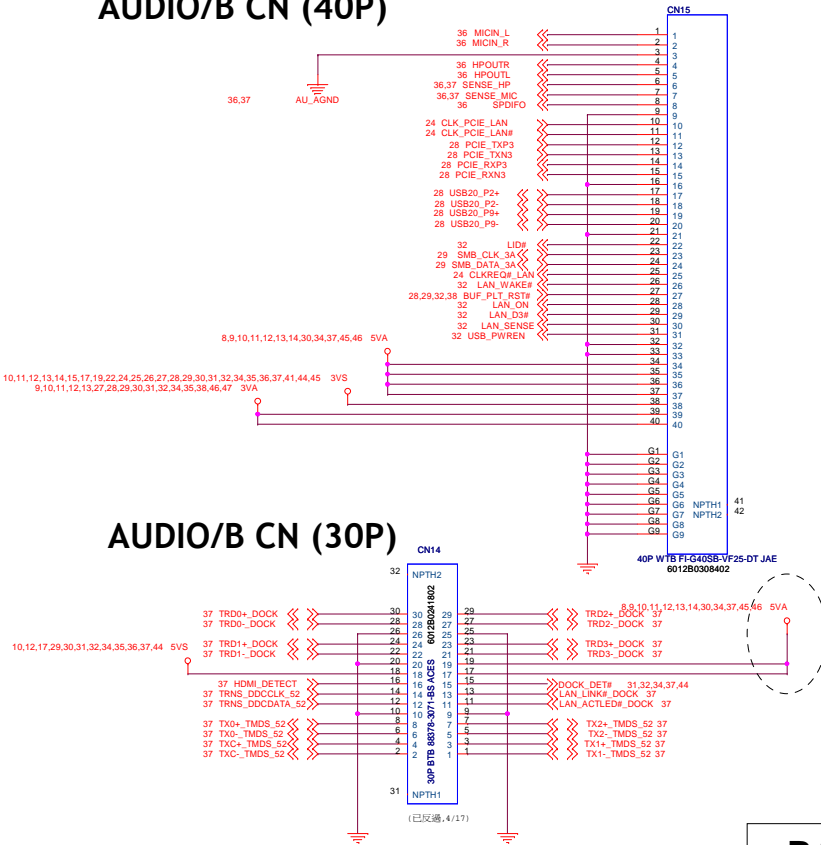
TITLE
BAP41/BAP51 (Montevina SFF)
LCD & CRT & CAM

SIZE	CODE	DOC. NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02

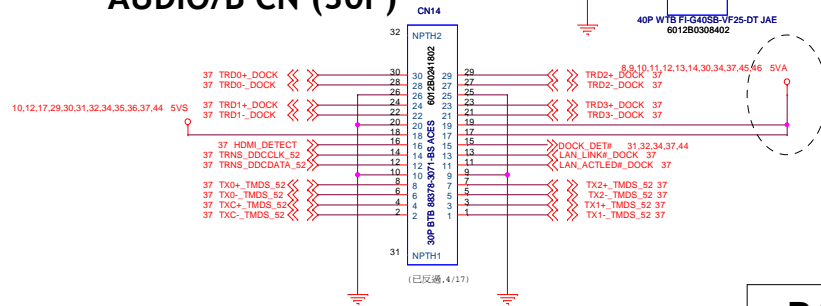
For Green PC



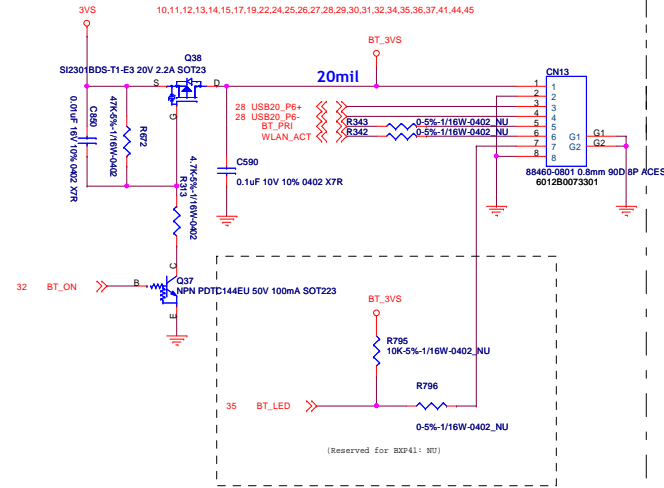
AUDIO/B CN (40P)



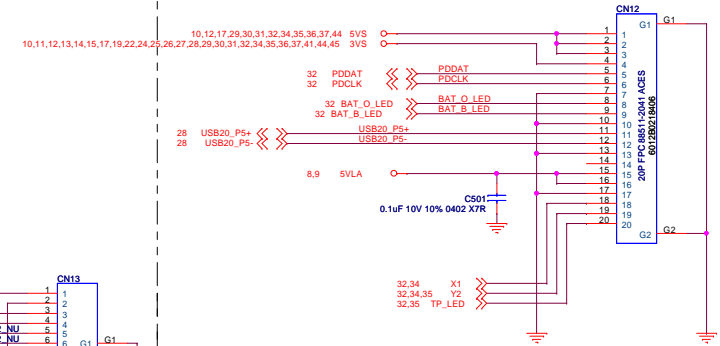
AUDIO/B CN (30P)



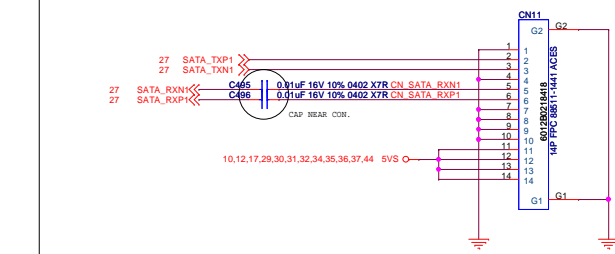
Bluetooth CN



GLIDE PAD Board



HDD BOARD CN

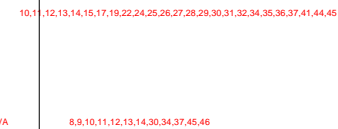
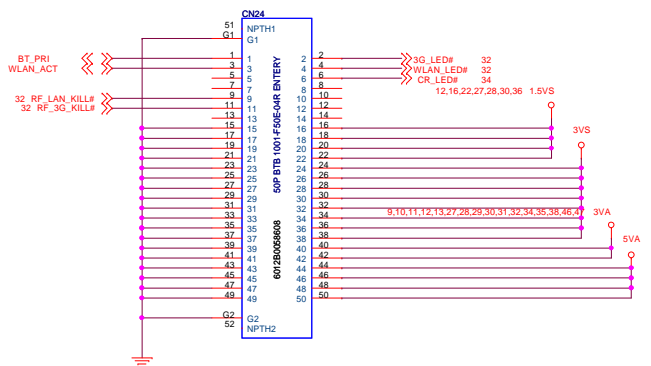


BAP41/BXP41: Transfer/B CN:6012B0058608

BAP51/52/SJM52: Mini-Card/B CN:6012B0058609

BAP41/BXP41: Transfer/B CN:6012B0058608

BAP51/52/SJM52: Mini-Card/B CN:6012B0058609



INVENTEC

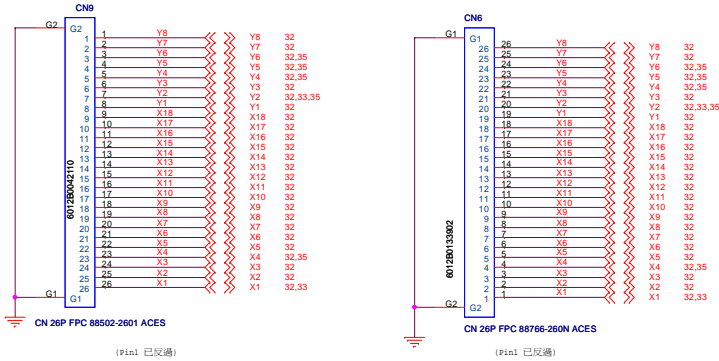
FILE: BAP41/BAP51 (Montevina SFF)

Daughter Connector

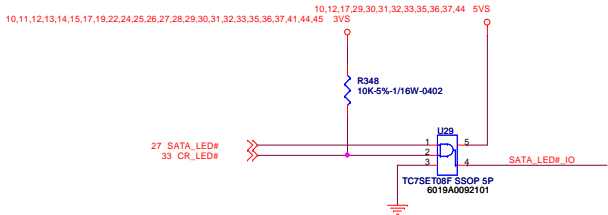
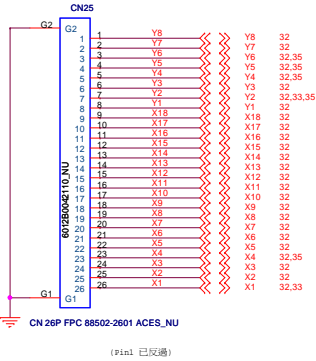
SIZE	CODE	DOC NUMBER	REV
Custom	A02	D-GS-1310A2292001-ALG	A02
SHEET		33	48

CHANGE by: Shun-Chin Chang DATE: Wednesday, July 01, 2009

To K/B(For BAP41) To K/B (For BAP51/BAP52/SJM52)

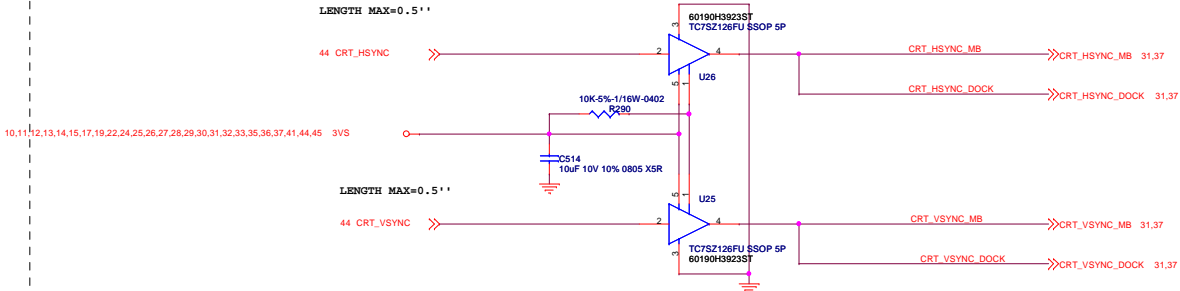
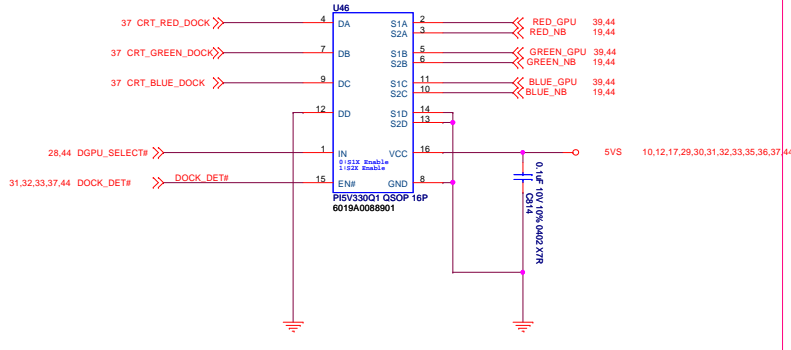


To K/B(For BXP41)

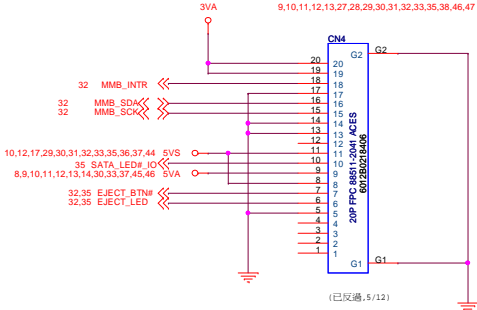


BAP41/51/52/BXP41: Stuff U46,C814

SJM52 : OPEN U46,C814

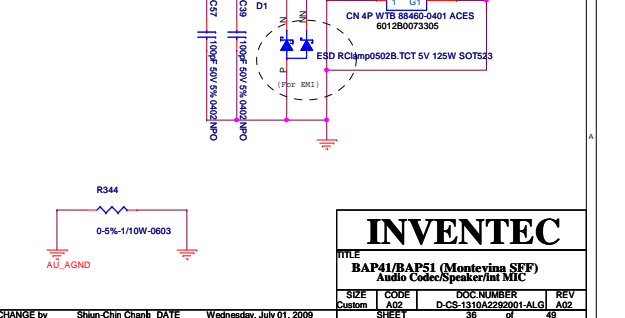
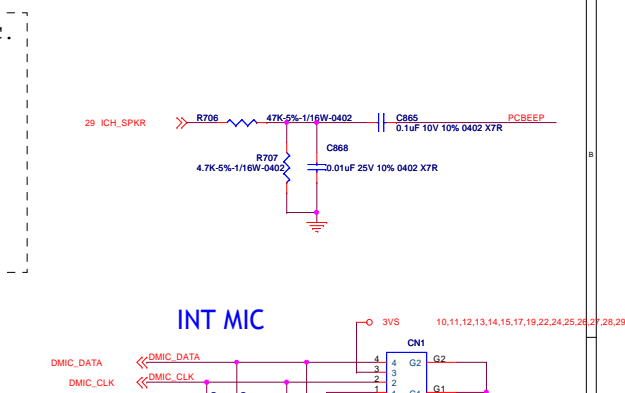
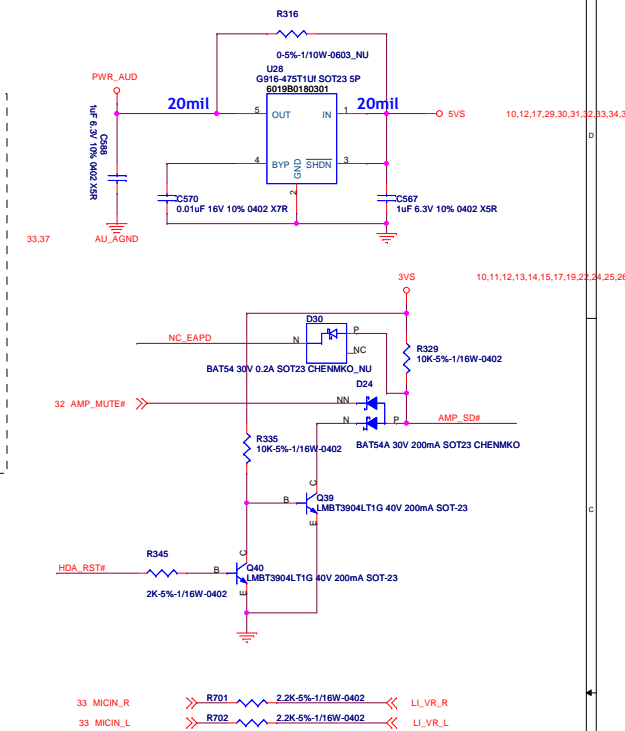


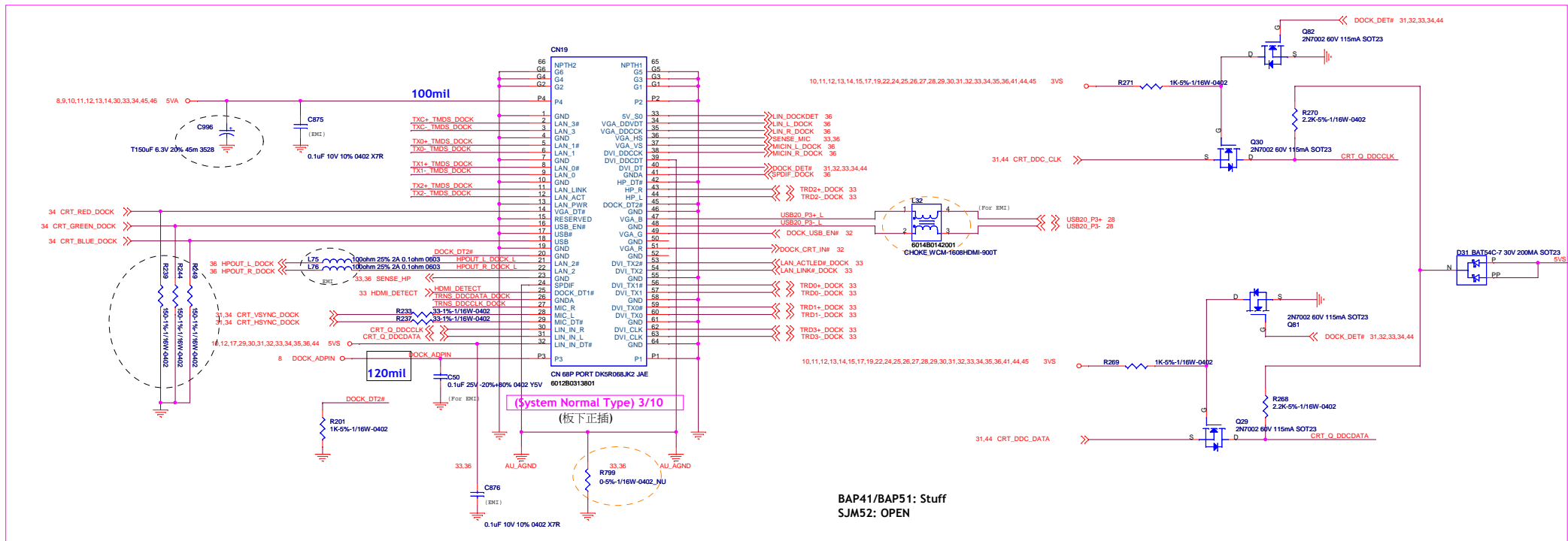
SW Sensor BOARD(For SJM52)



BAP41/51/52/BXP41: OPEN
SJM52: Stuff

INVENTEC			
BAP41/BAP51 (Montevina SFF) BDP			
SIZE	CODE	DOC NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02
SHEET 34 OF 48			



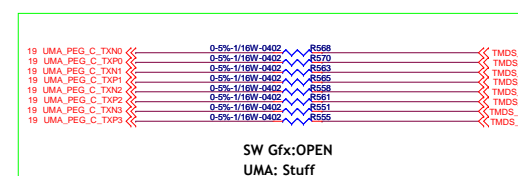
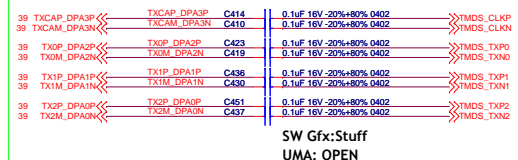


Layout Note: 2 components with one mutual pad, total 3 pads

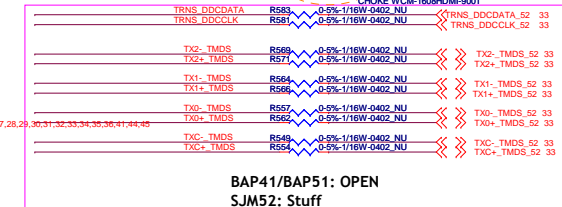
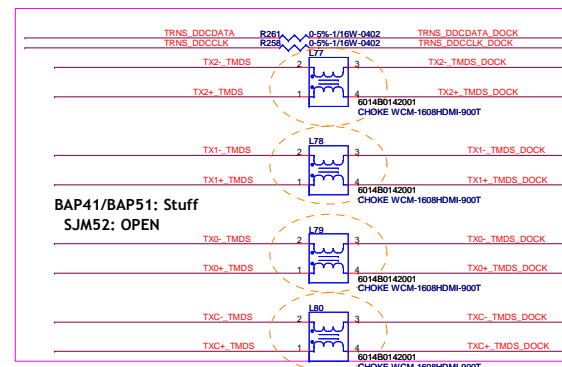
SW Gfx:OPEN, UMA: Stuff

SW Gfx:Stuff, UMA: OPEN

Place close to U16(PI3VDP411LSTZBEX)

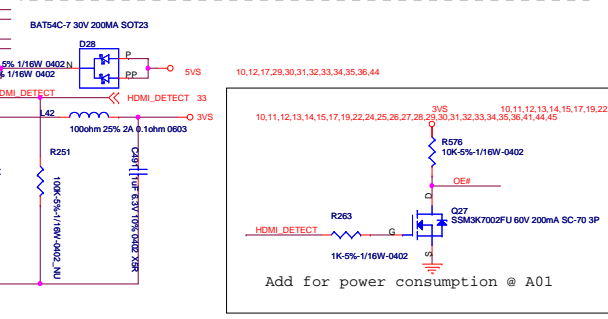
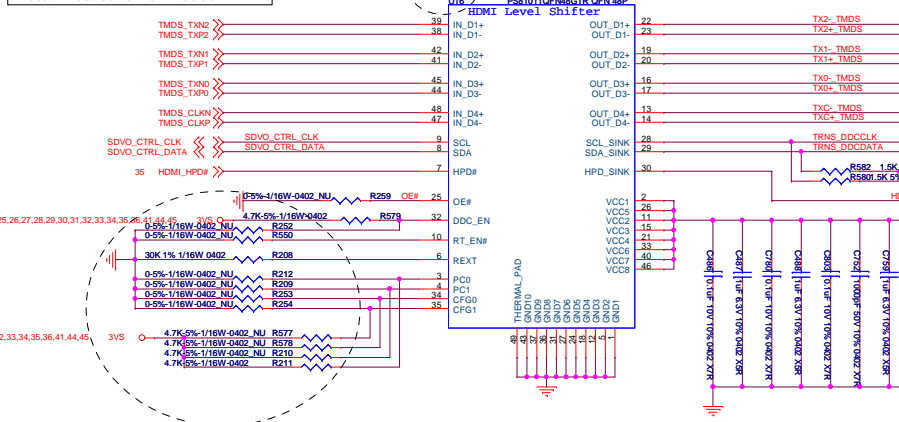


Place close to U16(PI3VDP411LSTZBEX)



Parade	Pericom
U16 : 6019B0585301	6019B0443802
R550 : OPEN	0 ohm
R208 : 30K	OPEN
R212 : OPEN	0 ohm
R209 : OPEN	0 ohm
R253 : OPEN	0 ohm
R577 : OPEN	4.7K
R211 : 4.7K	OPEN

Note: R208: SJM52 is not 30K



INVENTEC

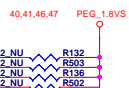
TITLE
BAP41/BAP51 (Montevina SFF)
EASY PORT CN-Level Shifter

SIZE CODE DOC NUMBER REV
Custom A02 D-CS-1310A220001-ALG A02

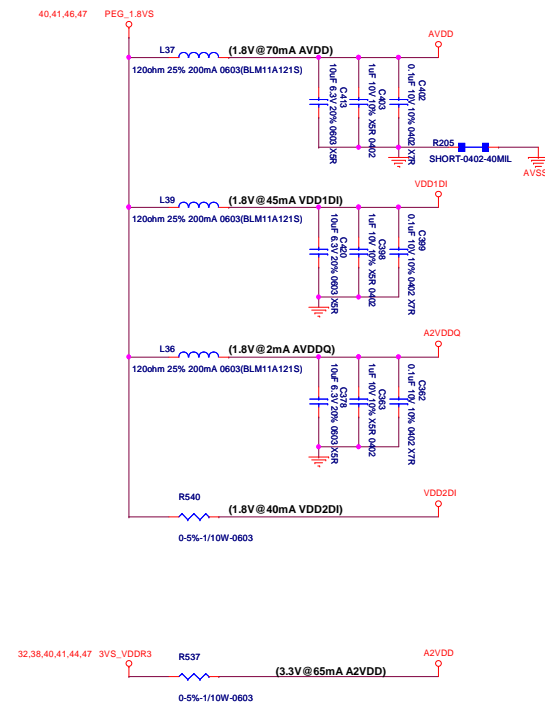
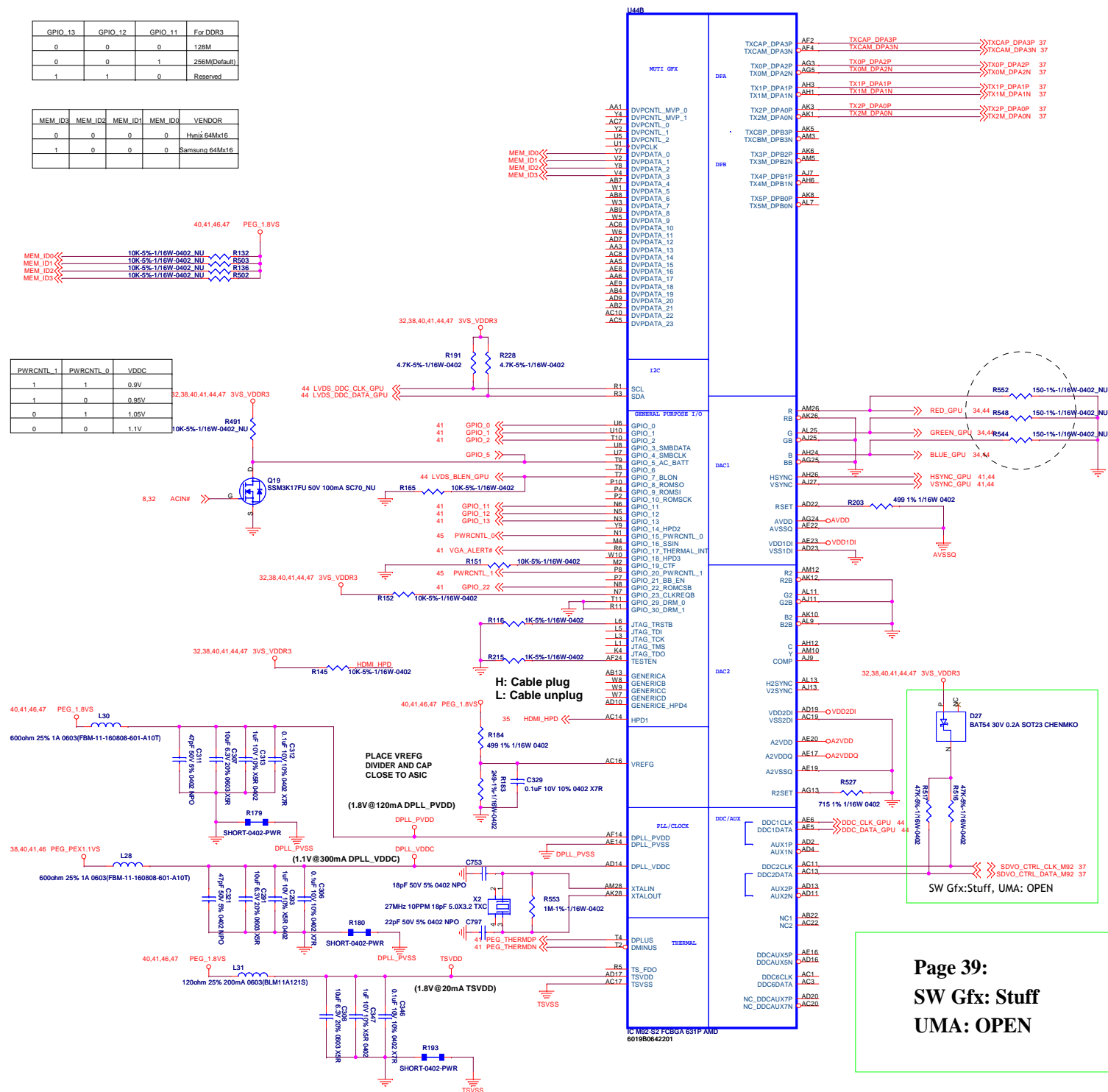
CHANGE by Shun-Chin Chang DATE Wednesday, July 01, 2009

SHEET 37 of 49

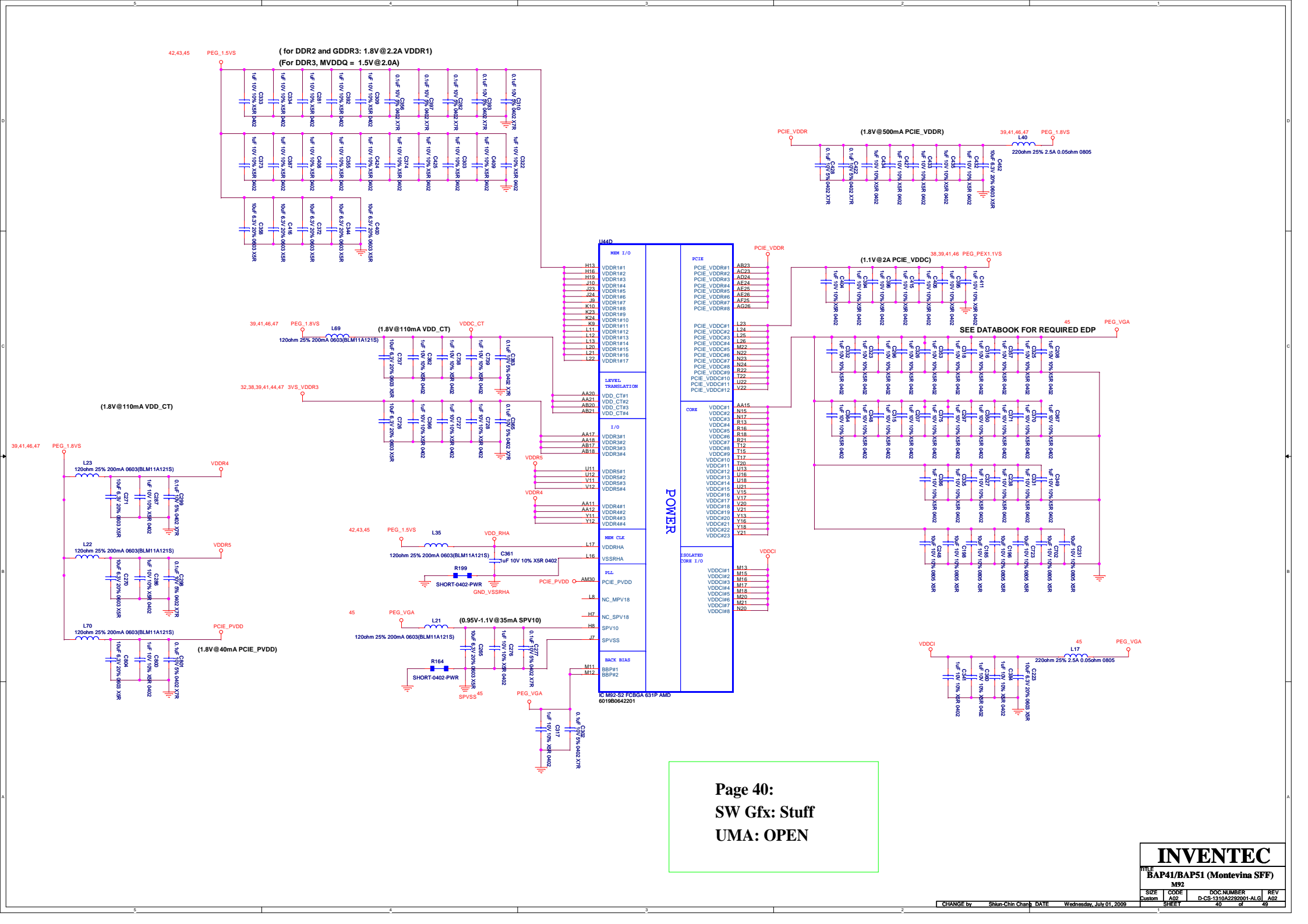
MEM ID3	MEM ID2	MEM ID1	MEM ID0	VENDOR
0	0	0	0	Hynix 64Mx16
1	0	0	0	Samsung 64Mx16



PWRCNTL_1	PWRCNTL_0	VDDC
1	1	0.9V
1	0	0.95V
0	1	1.05V
0	0	1.1V

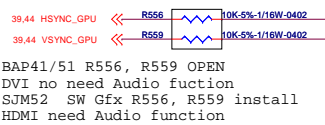
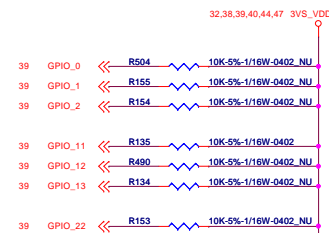
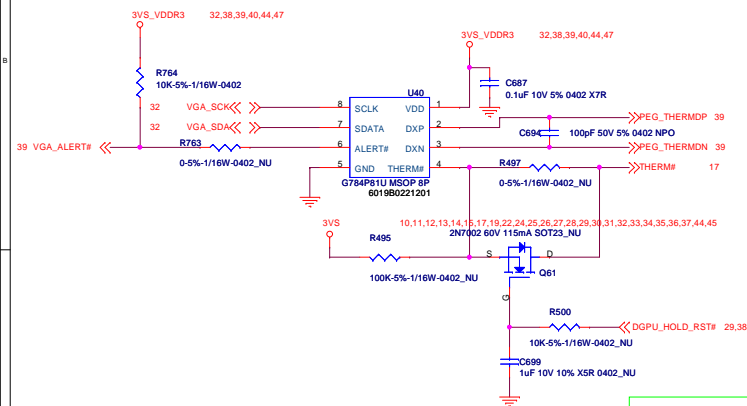
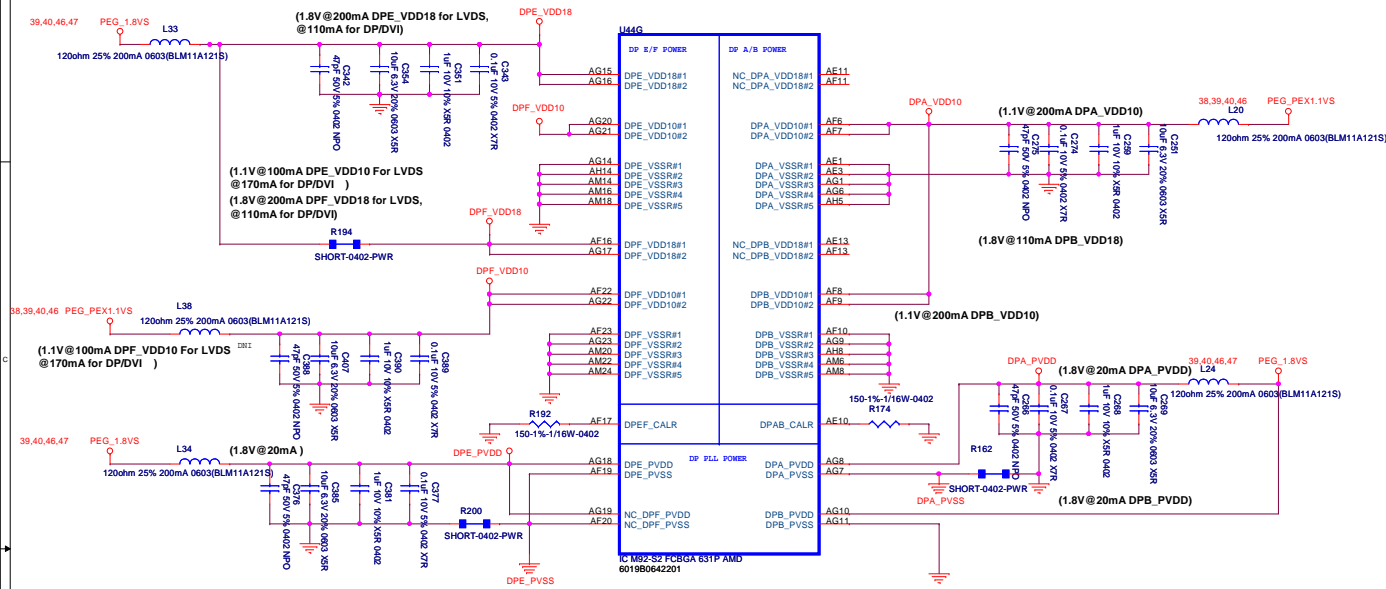


Page 39:
SW Gfx: Stuff
UMA: OPEN



Page 40:
SW Gfx: Stuff
UMA: OPEN

For 92, DPx_VDD10 = 1.1V
For Future ASIC, DPx_VDD10 = 1.0V



Page 41:
SW Gfx: Stuff
UMA: OPEN

PIN STRAPS

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
BIF_GEN2_EN_A	GPIO2	PCIE GEN2 ENABLED	X
RSVD	GPIO8		0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	X X X
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	X
RSVD	GENERICCC		0
AUD[1]	HSYNC	AUD[1] AUD[0]	0
AUD[0]	VSYN	0 0 No audio function	X X
		0 1 Audio for DisplayPort and HDMI if dongle is detected	
		1 0 audio for DisplayPort only	
		1 1 Audio for both DisplayPort and HDMI	

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

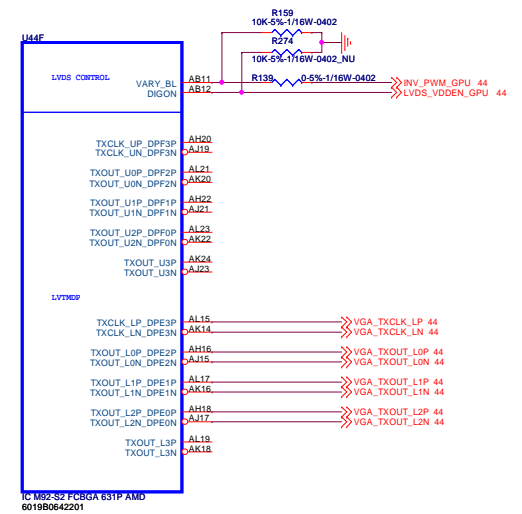
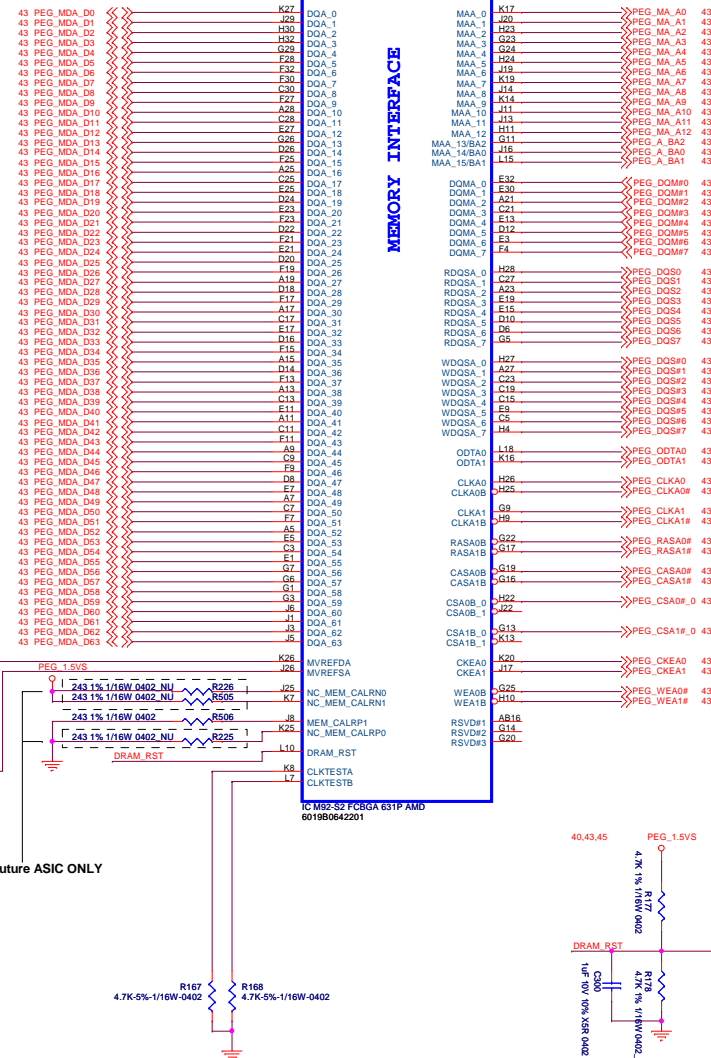
H2SYNC	GENERICC
<p>PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET</p>	
GPIOD1_BB_EN	

INVENTEC

TITLE
BAP41/BAP51 (Montevina SFF)
M92

CHANGE by	Shiun-Chin Chang	DATE	Wednesday, July 01, 2009
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U44C



**PLACE MVREF DIVIDERS
AND CAPS CLOSE TO ASIC**

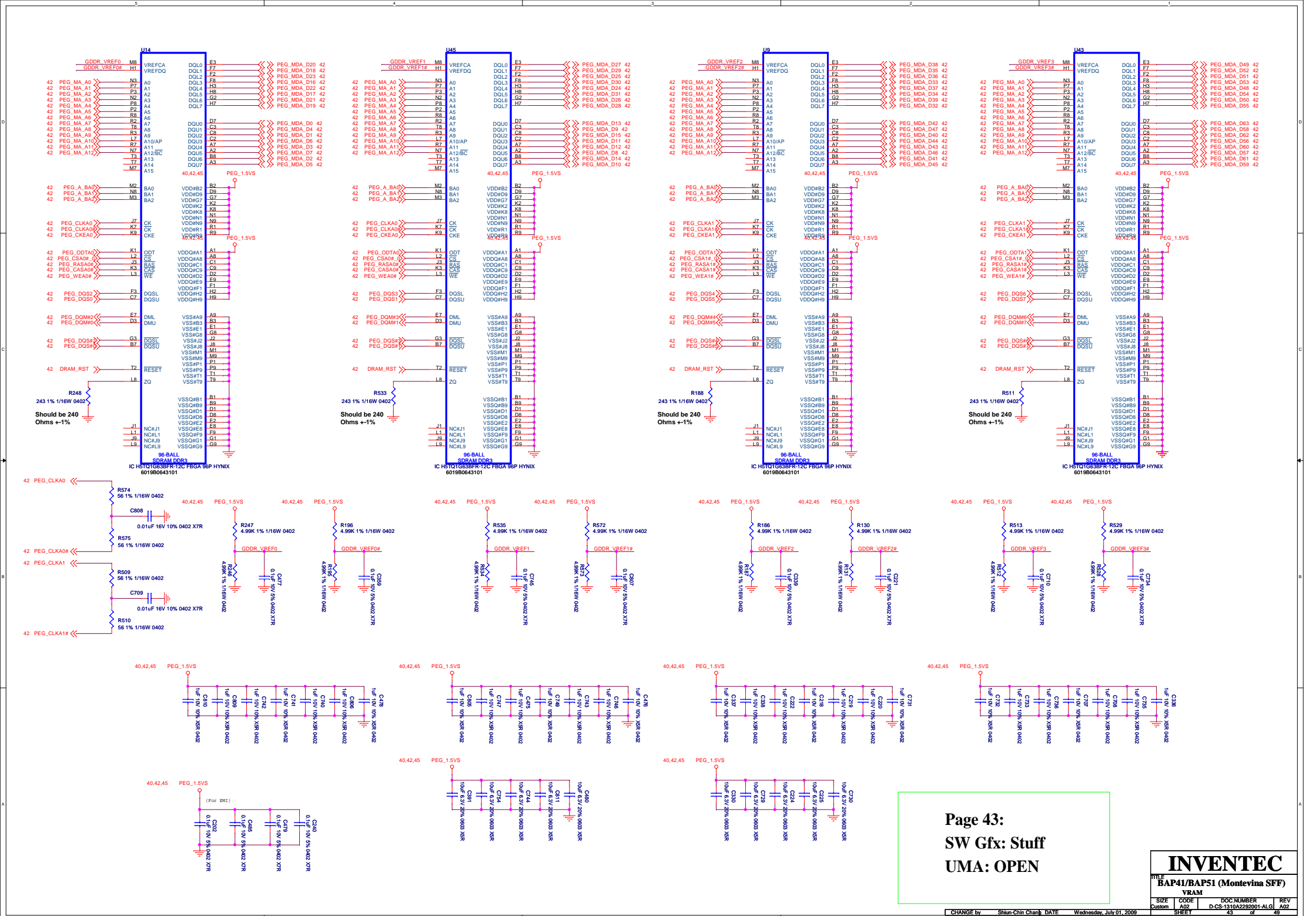
DIVIDER RESISTORS	DDR2/DDR3	GDDR3
MVREF TO 1.8V (Ra)	100R	40.2R
MVREF TO GND (Rb)	100R	100R

DNI, FOR Future ASIC ONLY

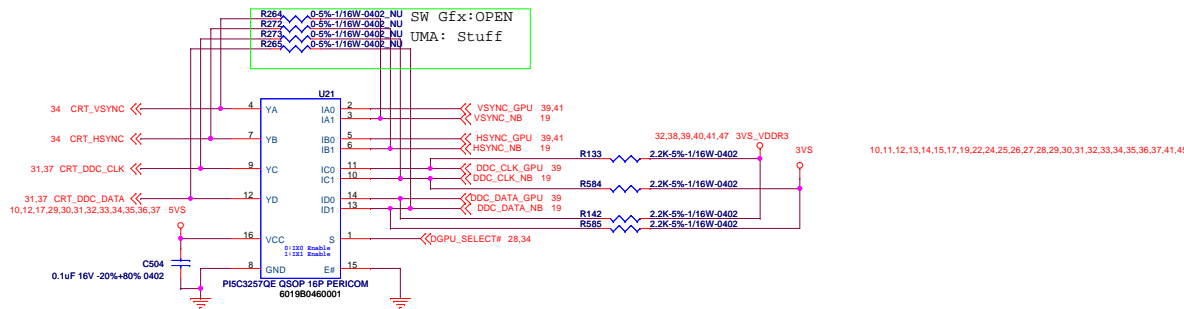
Page 42:
SW Gfx: Stuff
UMA: OPEN

INVENTEC

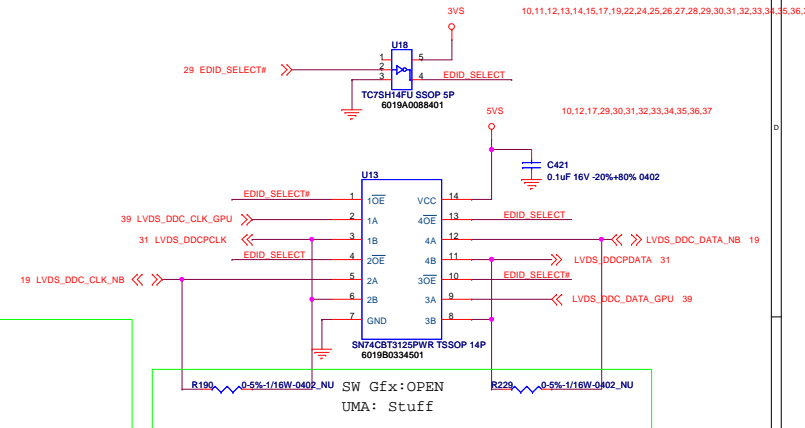
TITLE			
BAP41/BAP51 (Montevina SFF)			
M92			
SIZE	CODE	DOC NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02
SHEET		42	of 49



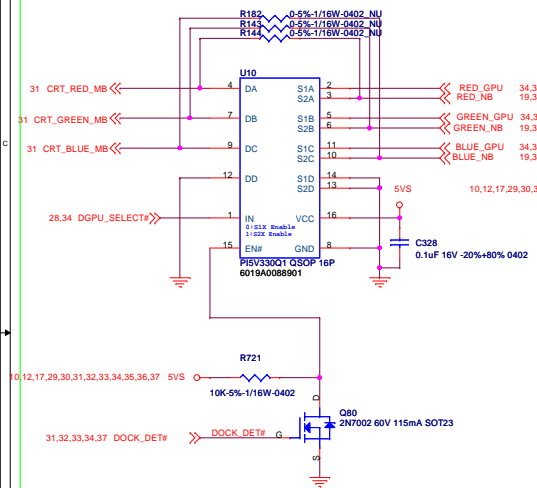
CRT HSYNC/VSNC/DDC SW



LCD DDC SW



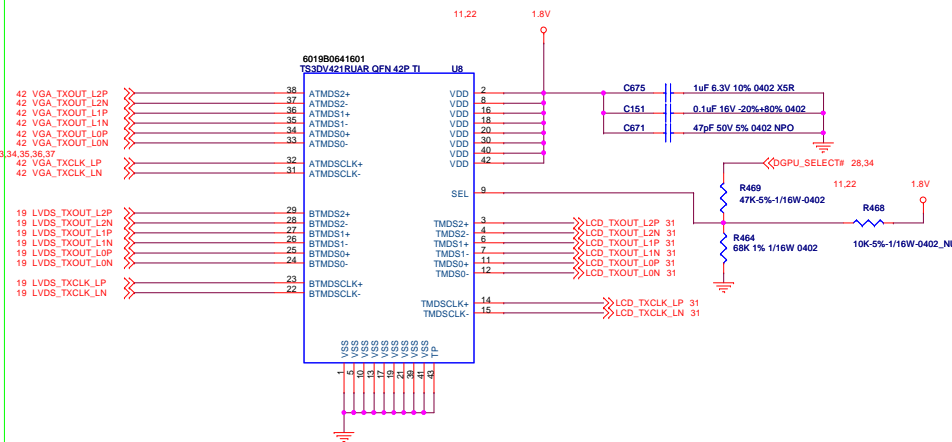
CRT R/G/B SW



Stuff CRT/RGB SW for both SW Gfx and UMA

SW Gfx : Stuff U10,C328,R721,Q80
UMA : Stuff U10,C328,R721,Q80

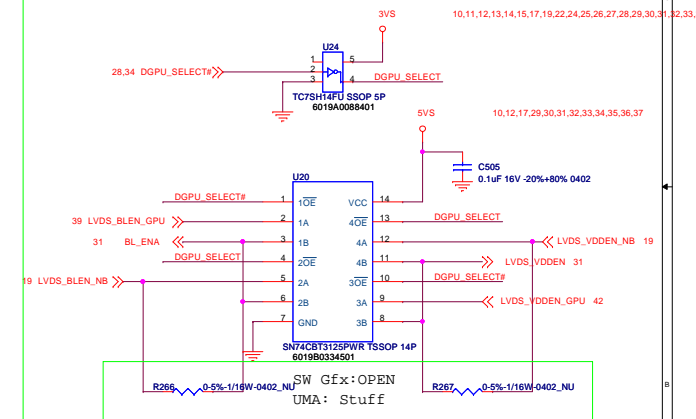
LVDS SW



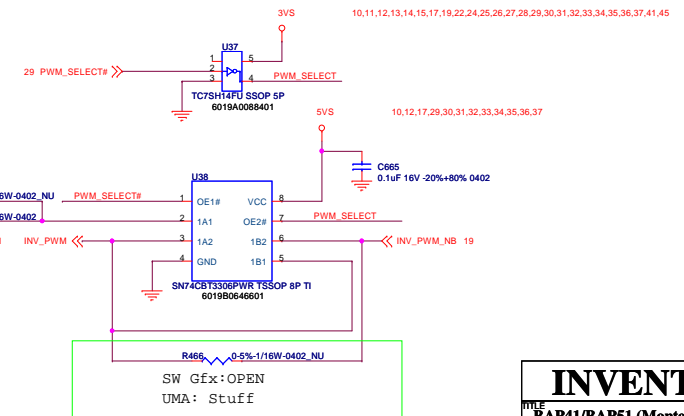
Thermal Pad limitation : Stuff LVDS SW for both SW Gfx and UMA

SW Gfx : Stuff U8,C675,C151,C671,R469,R464, OPEN R468
UMA : Stuff U8,C675,C151,C671,R468, OPEN R469,R464

LVDS BKL and Vcc Enable SW



LCD PWM SW

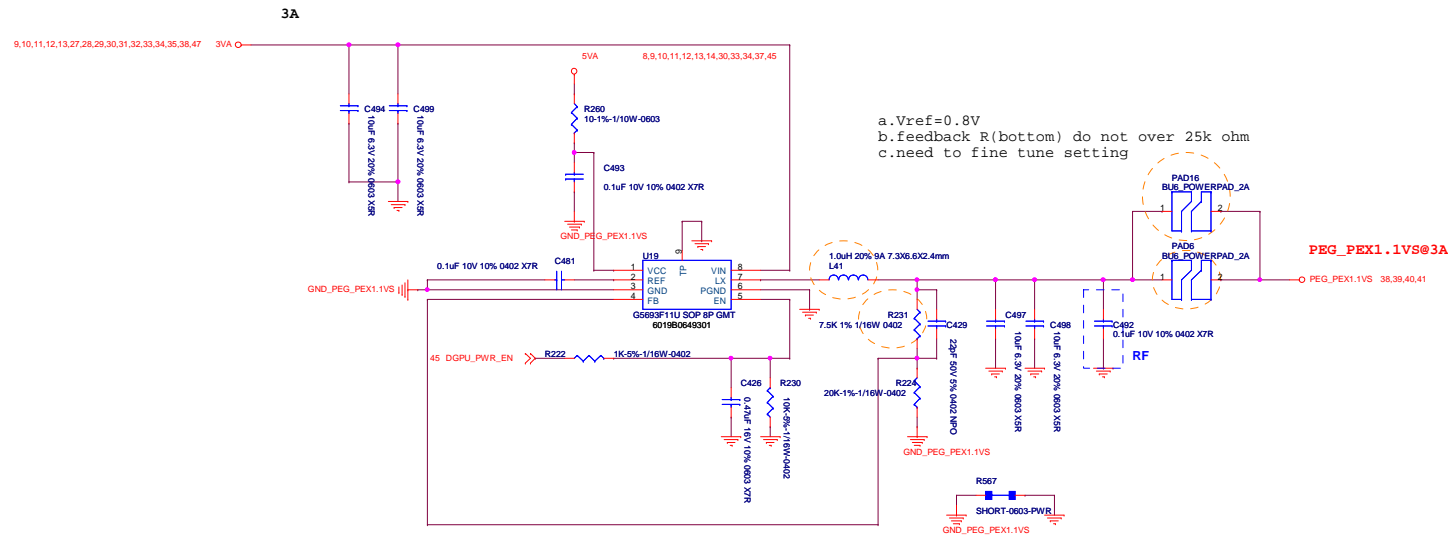
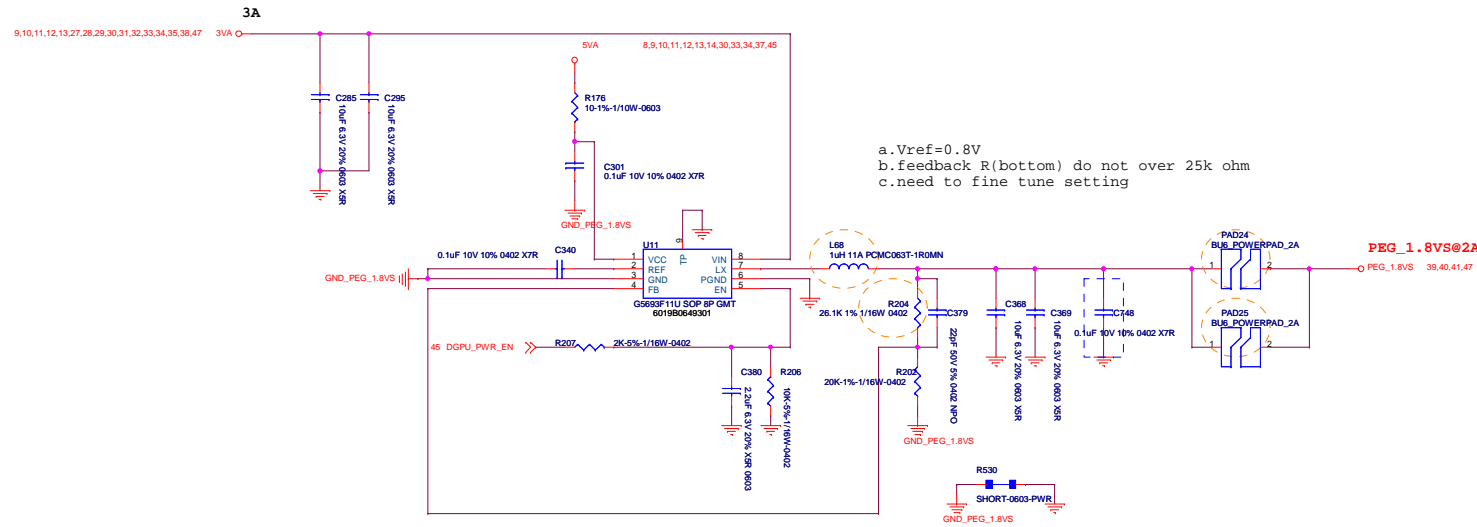


Page 44:
SW Gfx: Stuff
UMA: OPEN

INVENTEC
BAP41/BAP51 (Montevina SFF)
Hybrid switch

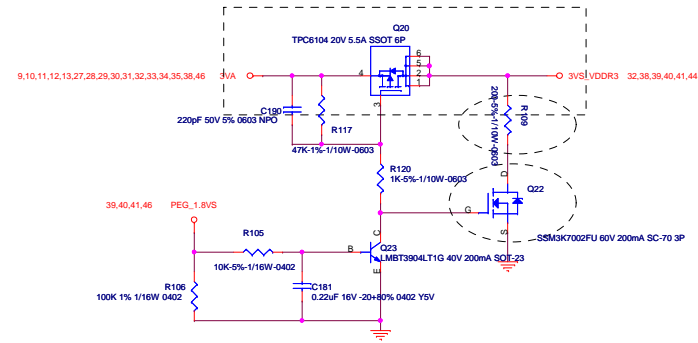
SIZE	CODE	DOC NUMBER	REV
Custom	A02	D-CS-1310A222001-ALG	A02
SHEET		44	of 48

CHANGE by: Shun-Chin Chang DATE: Wednesday, July 01, 2009



Page 46:
SW Gfx: Stuff
UMA: OPEN

INVENTEC				
TITLE BAP41/BAP51 (Montevina SFF)				
VGA Power				
SIZE	CODE	DOC NUMBER	REV	
Custom	A02	D-CS-1310A2290001-ALG	A02	
SHEET		49	of	

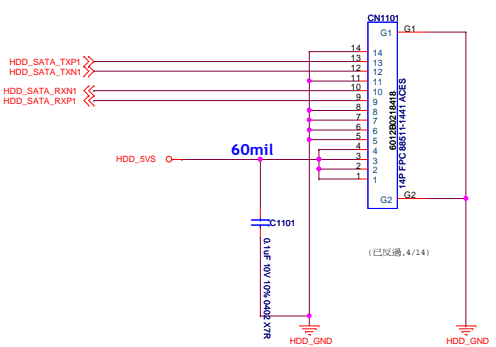


Page 47:
SW Gfx: Stuff
UMA: OPEN

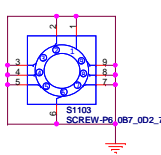
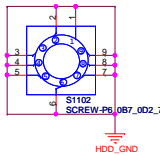
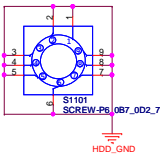
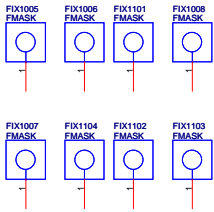
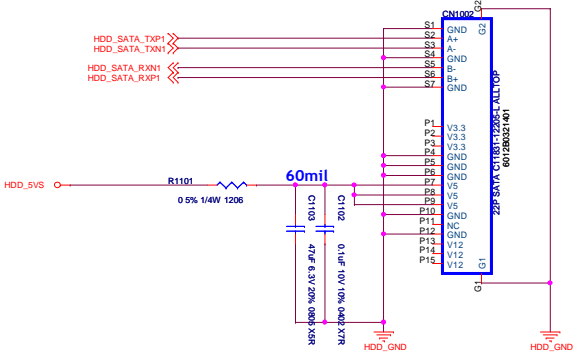
INVENTEC				
TITLE BAP41/BAPS1 (Montevina SFF) VGA Power				
SIZE	CODE	DOC. NUMBER		REV
Custom	A02	D-CS-1310A229001-ALG		A02
SHEET		47	of	49

CHANGE by Shun-Chin Chang DATE Wednesday, July 01, 2009

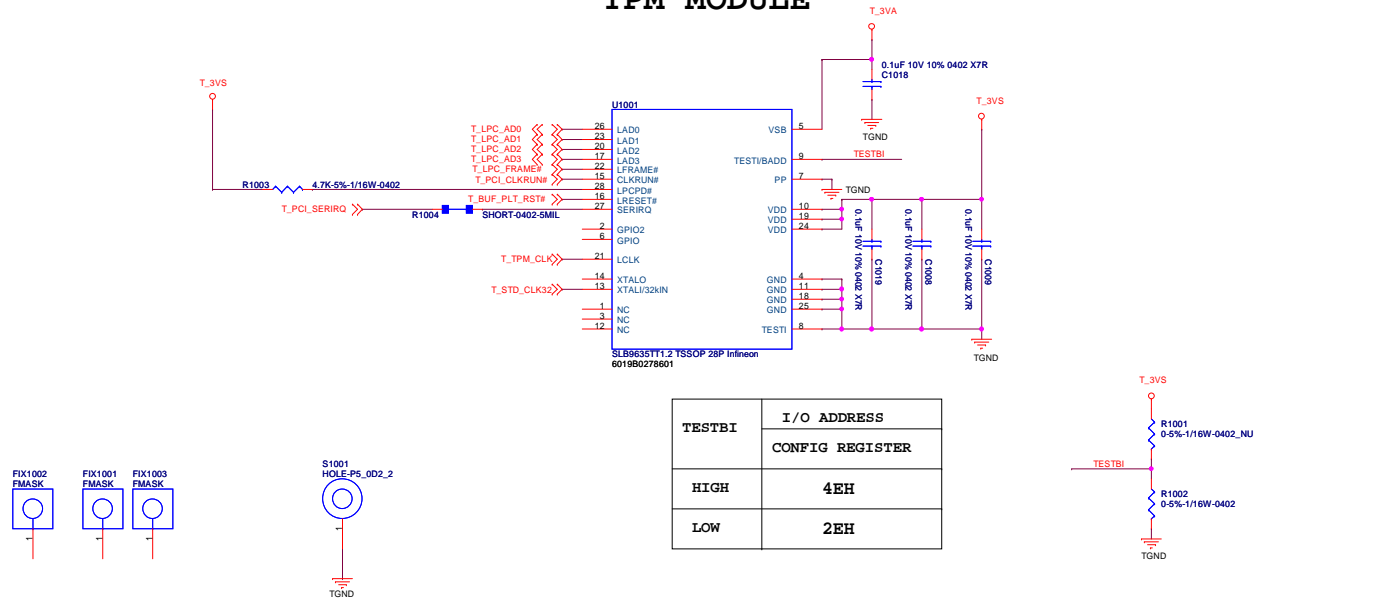
HDD Board CN TO MB



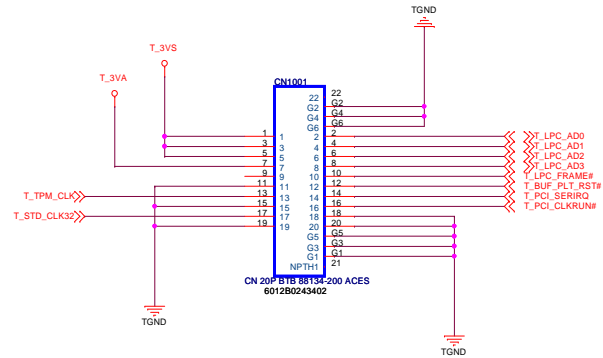
HDD I/F



TPM MODULE



TO MINI-CARD/B



INVENTEC

TITLE	BAP41/BAP51 (Montevina SFF) TPM Board
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SIZE	CODE	DOC. NUMBER	REV
Custom	A02	D-CS-1310A2292001-ALG	A02
SHEET		49	of 49